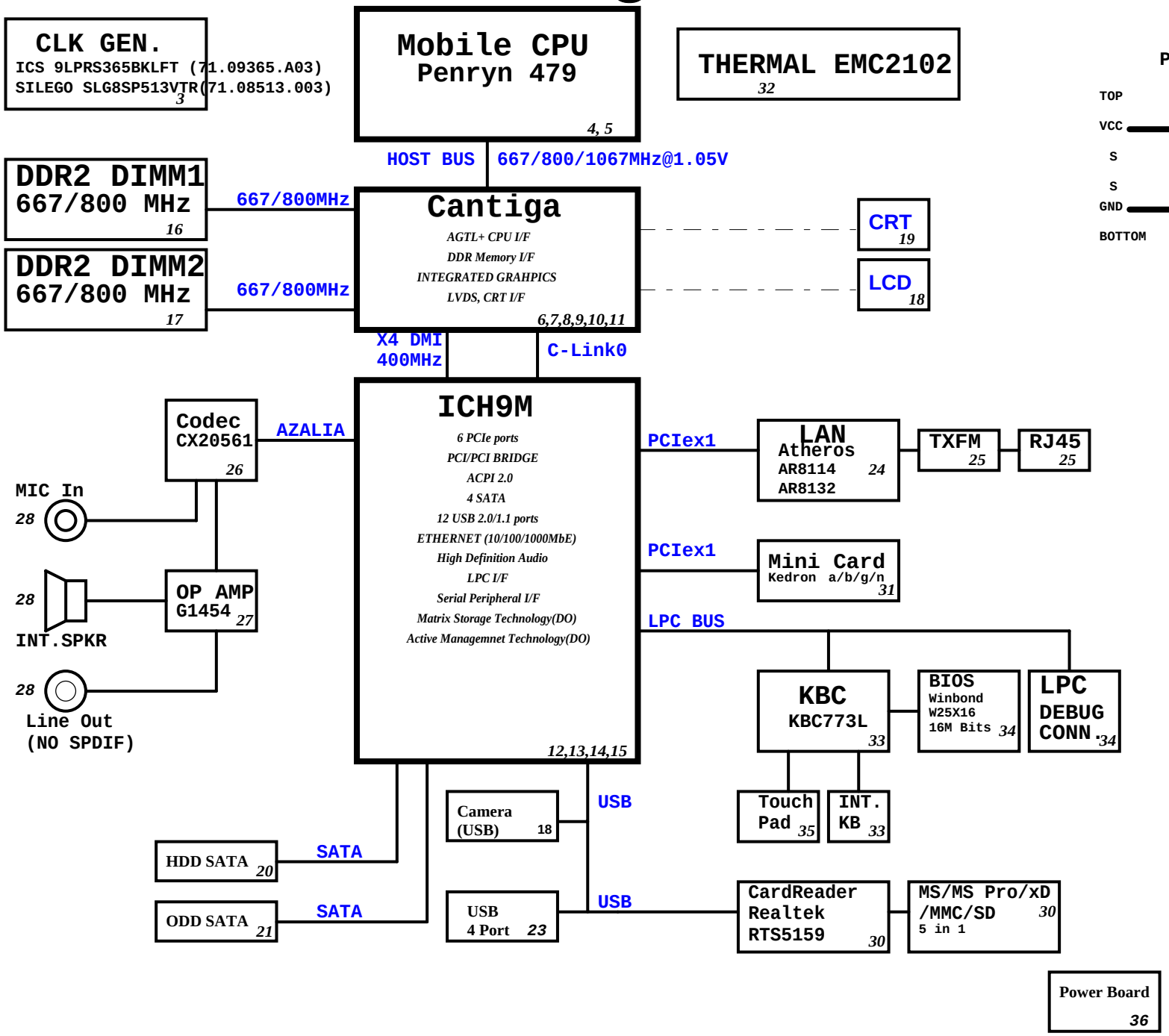
LA14 Block Diagram

Project code: 91.4BW01.001
PCB P/N : 48.4BW01.01M
REVISION : SA



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
TPS51125 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
TPS51124 44

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 43

1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 43

1D8V_S3	1D5V_S0

CPU DC/DC
ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER
BQ24745 46

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

<Core Design>

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	LA14	SB

Date: Thursday, May 07, 2009 Sheet 1 of 52

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

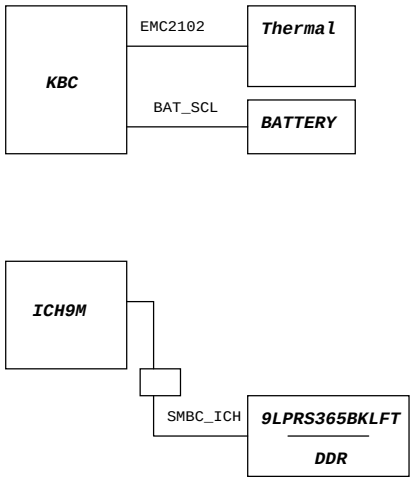
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



USB Table

USB	
Pair	Device
0	USB1
1	NC
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB2(High speed)
10	NC
11	CardReader

PCIE Routing

LANE1	LAN Atheros AR8114A
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

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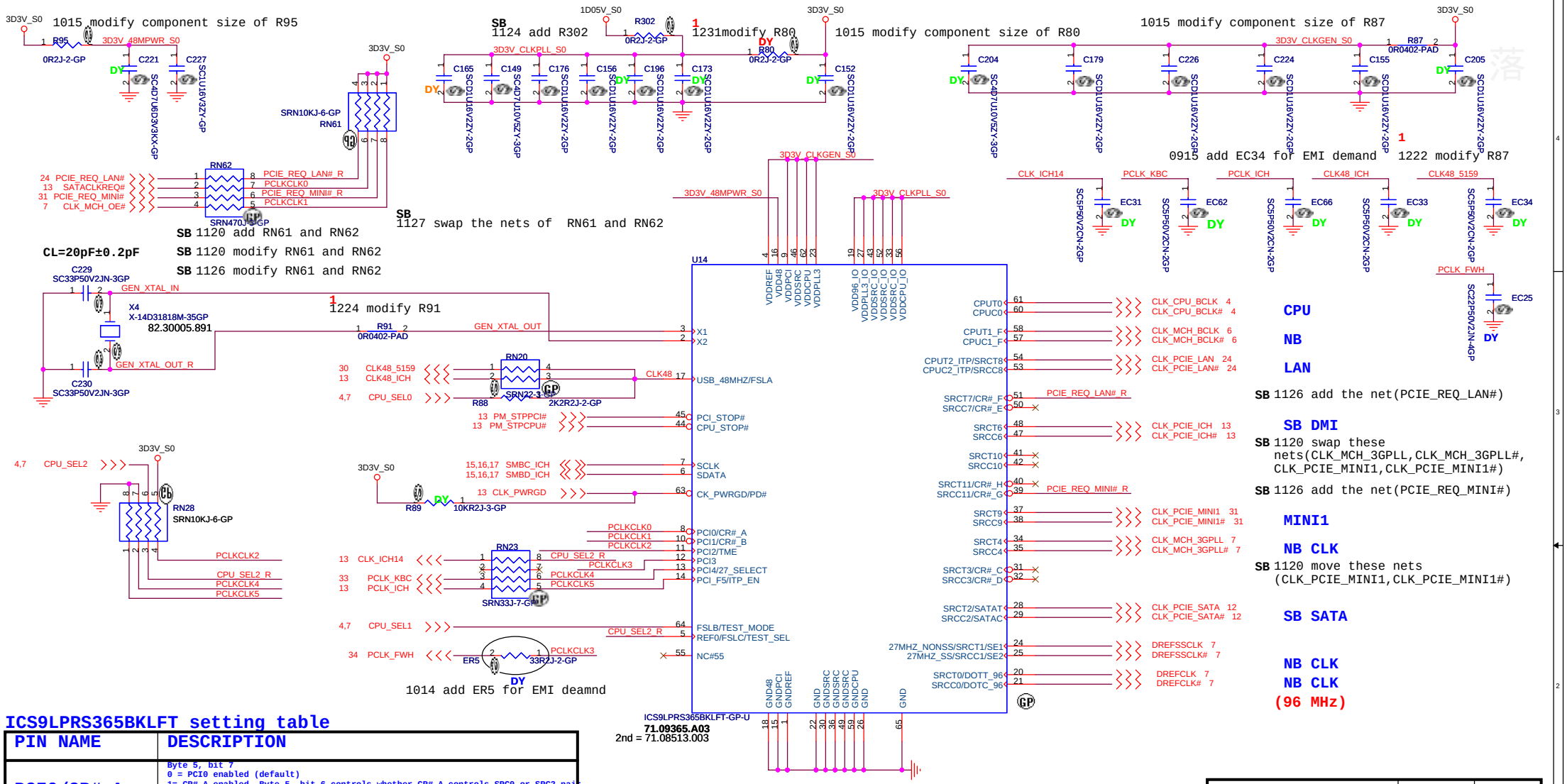
Title: Reference

Size: A3 | Document Number: LA14 | Rev: SB

Date: Thursday, May 07, 2009 | Sheet 2 of 52



ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

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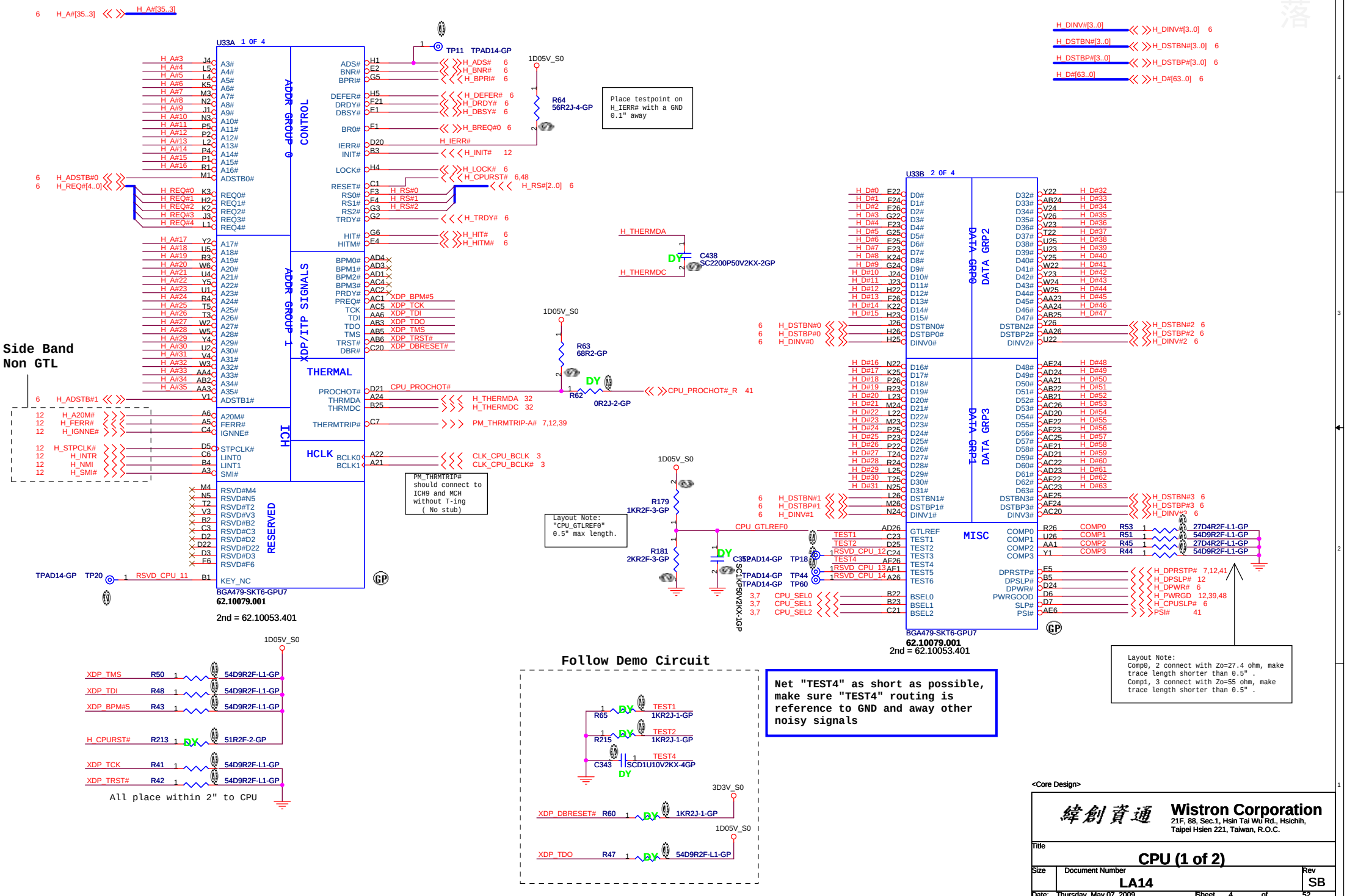
U33A 1 0F 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
Side Band
Non GTL
TP11 TPAD14-GP
1D05V_S0
R64 56R2J-4-GP
Place testpoint on H_IERR# with a GND 0.1" away
H_THERMDA
H_THERMDC
C438 SC2200P50V2KX-2GP
R63 68R2-GP
R62 0R2J-2-GP
CPU_PROCHOT#_R 41
PM_THRMTRIP-A# 7,12,39
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
R179 1KR2F-3-GP
R181 2KR2F-3-GP
CPU_GTLREF0
Layout Note: "CPU_GTLREF0" 0.5" max length.
TPAD14-GP TP20
RSVD_CPU_11
U33B 2 0F 4
DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
H_DINV#[3..0]
H_DSTBN#[3..0]
H_DSTBP#[3..0]
H_D#[63..0]
27D4R2F-L1-GP
54D9R2F-L1-GP
H_DPRSTP# 7,12,41
H_DPSLP# 12
H_DPWR# 6
H_PWRGD 12,39,48
H_CPUSLP# 6
PSI# 41
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
XDP_TMS R50 54D9R2F-L1-GP
XDP_TDI R48 54D9R2F-L1-GP
XDP_BPM#5 R43 54D9R2F-L1-GP
H_CPURST# R213 51R2F-2-GP
XDP_TCK R41 54D9R2F-L1-GP
XDP_TRST# R42 54D9R2F-L1-GP
All place within 2" to CPU
Follow Demo Circuit
R65 TEST1 1KR2J-1-GP
R215 TEST2 1KR2J-1-GP
C343 SCD1U10V2KX-4GP TEST4
3D3V_S0
XDP_DBRESET# R60 1KR2J-1-GP
XDP_TDO R47 54D9R2F-L1-GP
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
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Title
CPU (1 of 2)
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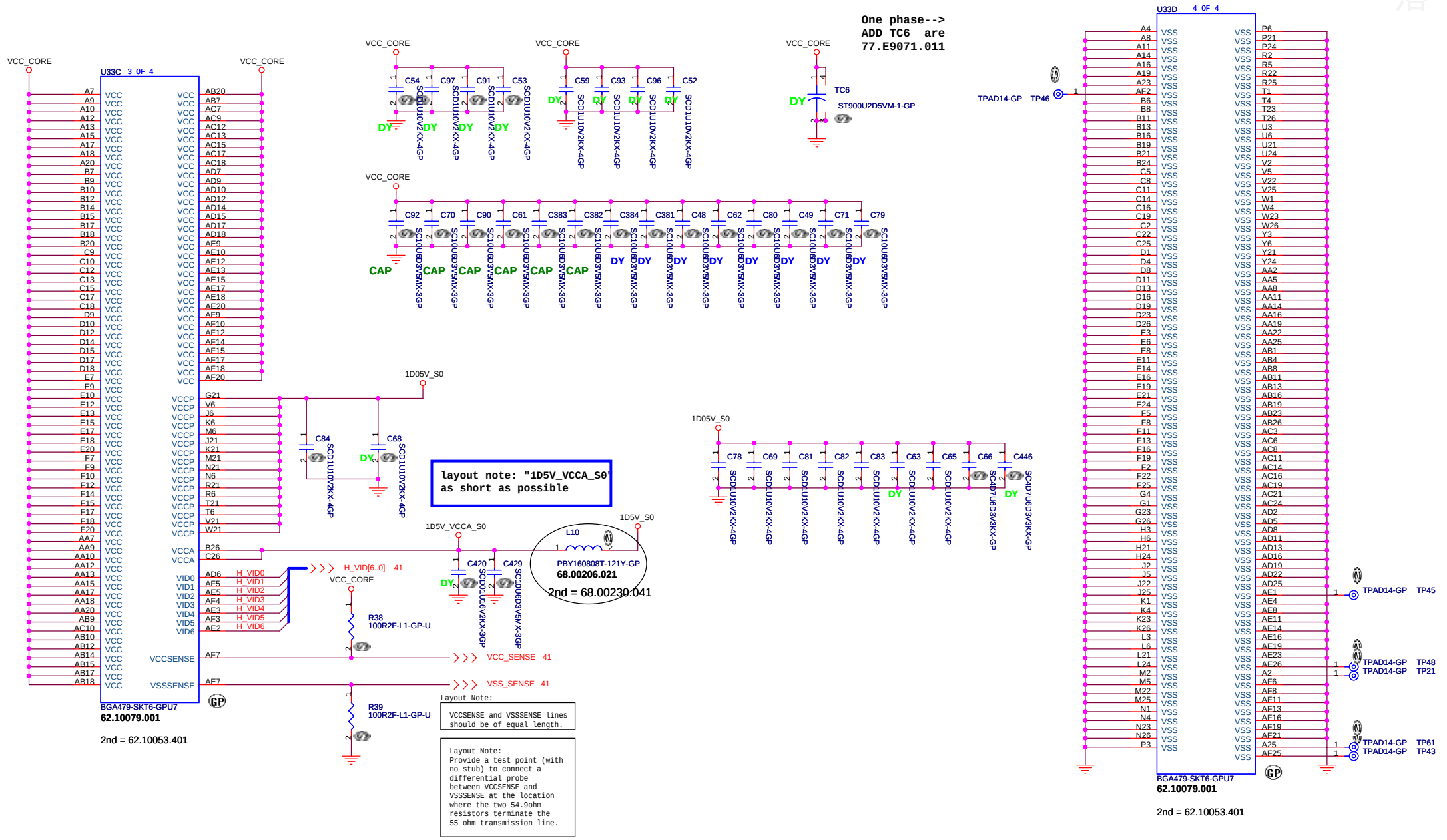

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Title	CPU (2 of 2)	
Size	Document Number: LA14	Rev: SB
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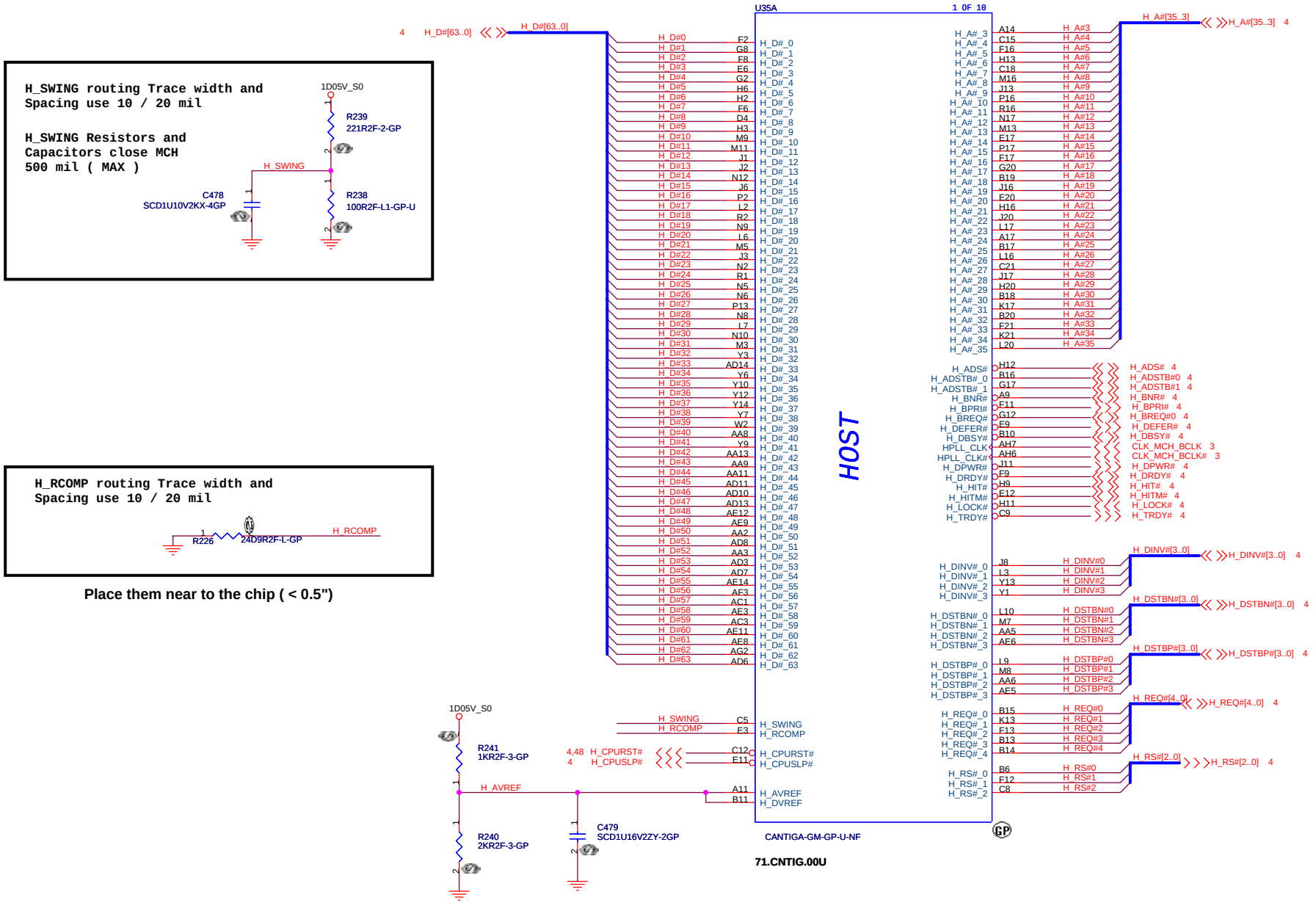

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Title: **Cantiga (1 of 6) HOST**

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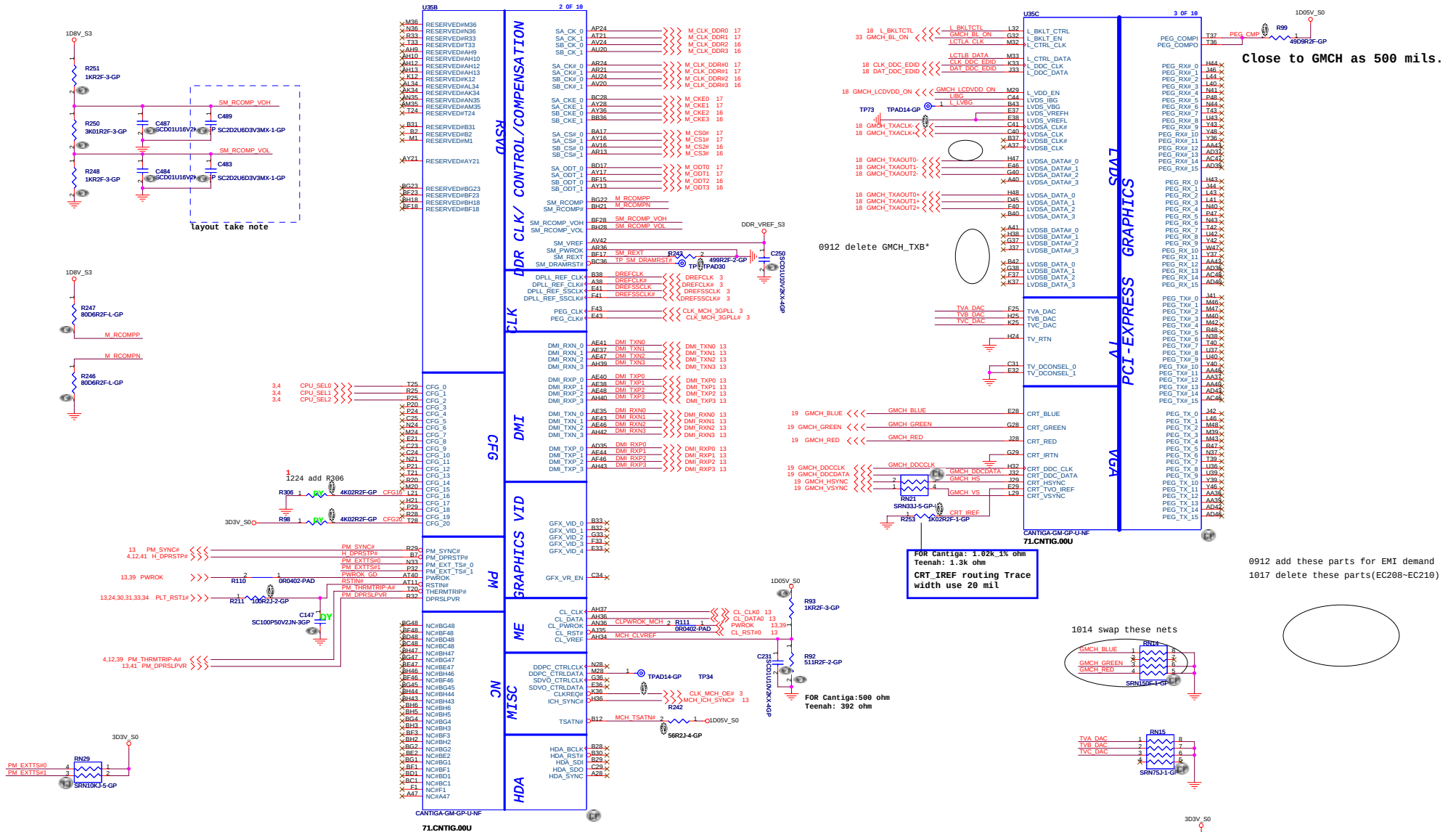

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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Title: Cantiga (2 of 6)_DMI/PM/CFG

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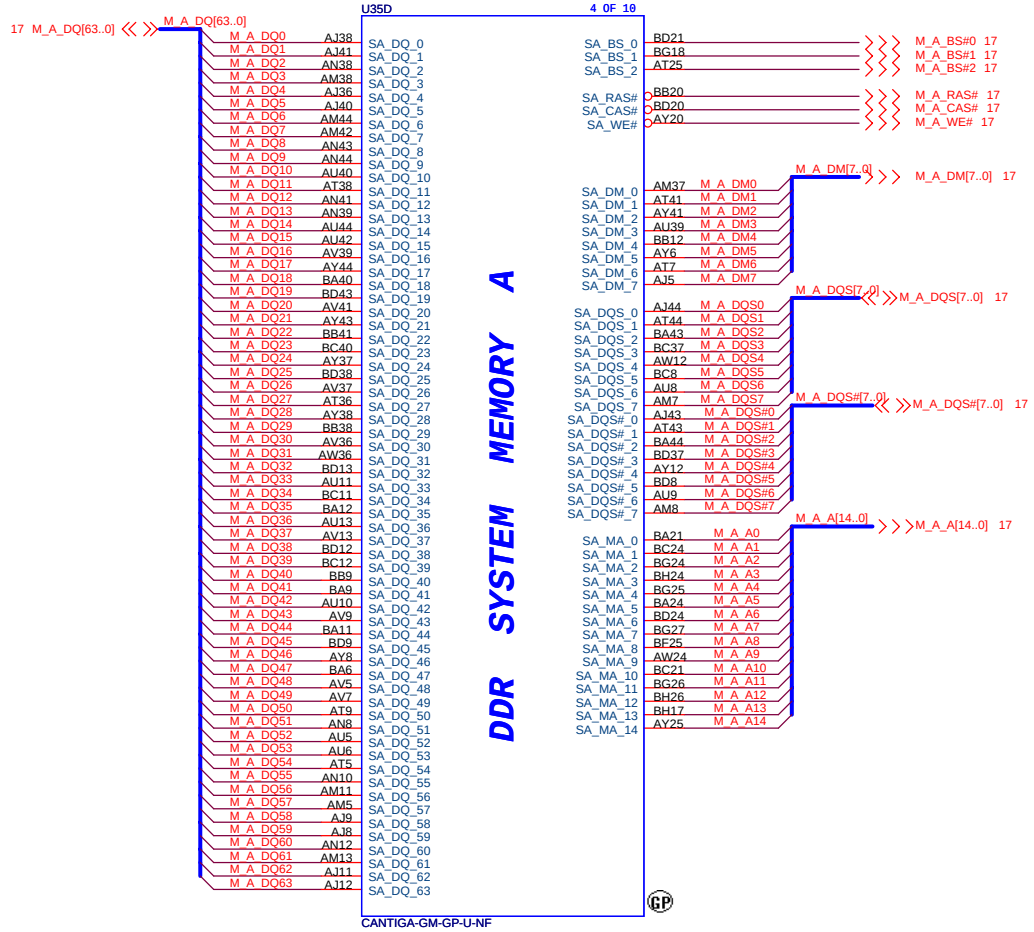

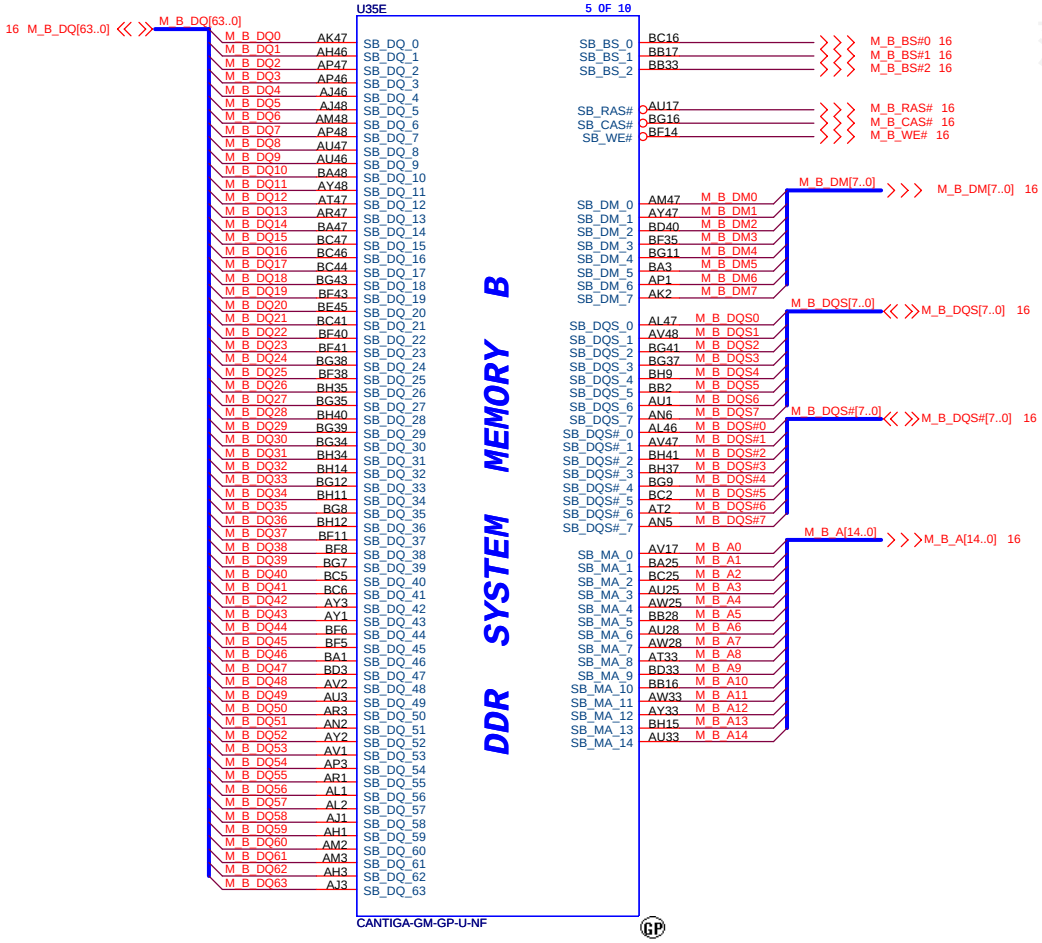

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Title: **Cantiga (3 of 6) DDR**

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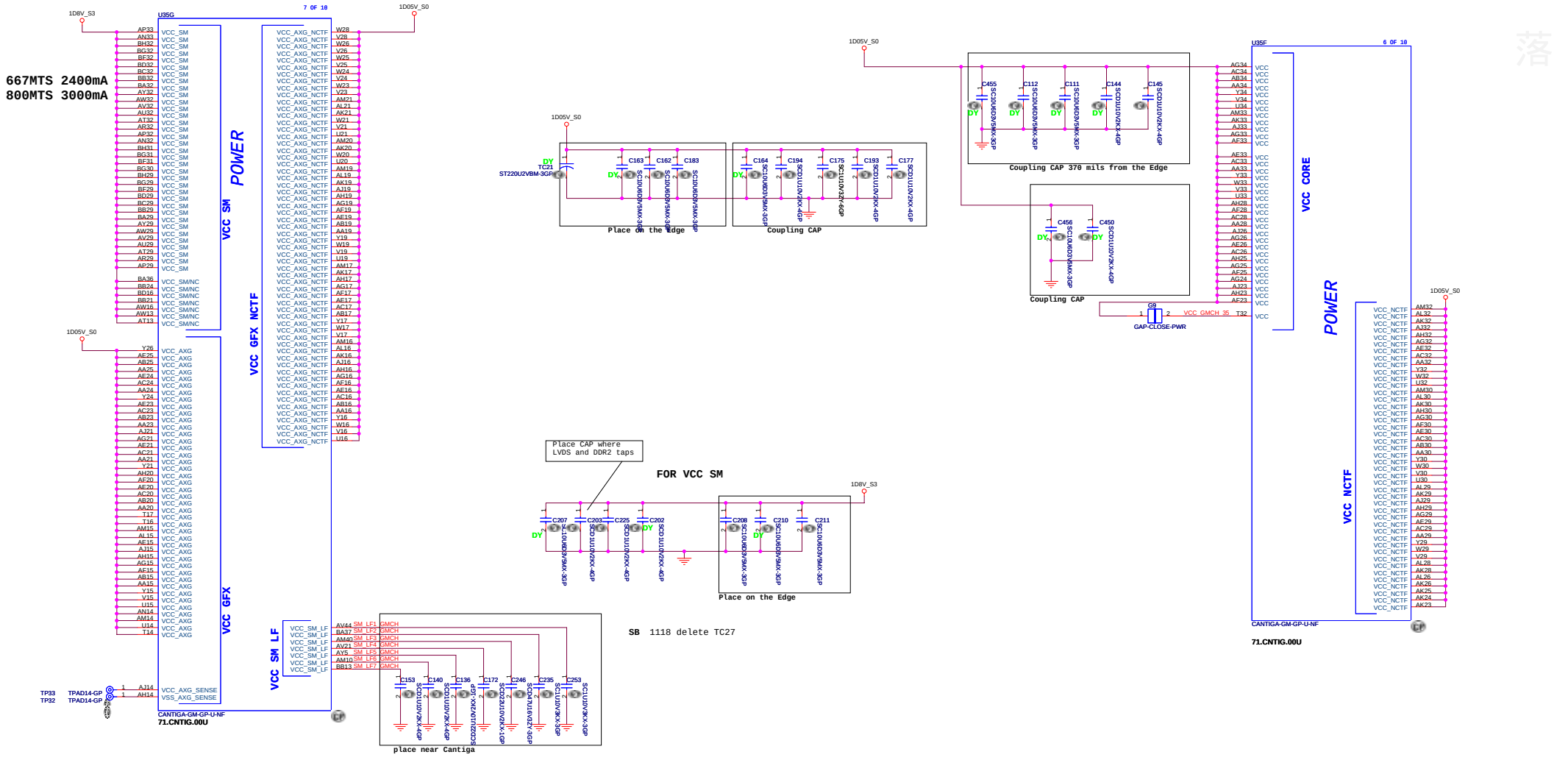

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Title: Cantiga (4 of 6) POWER

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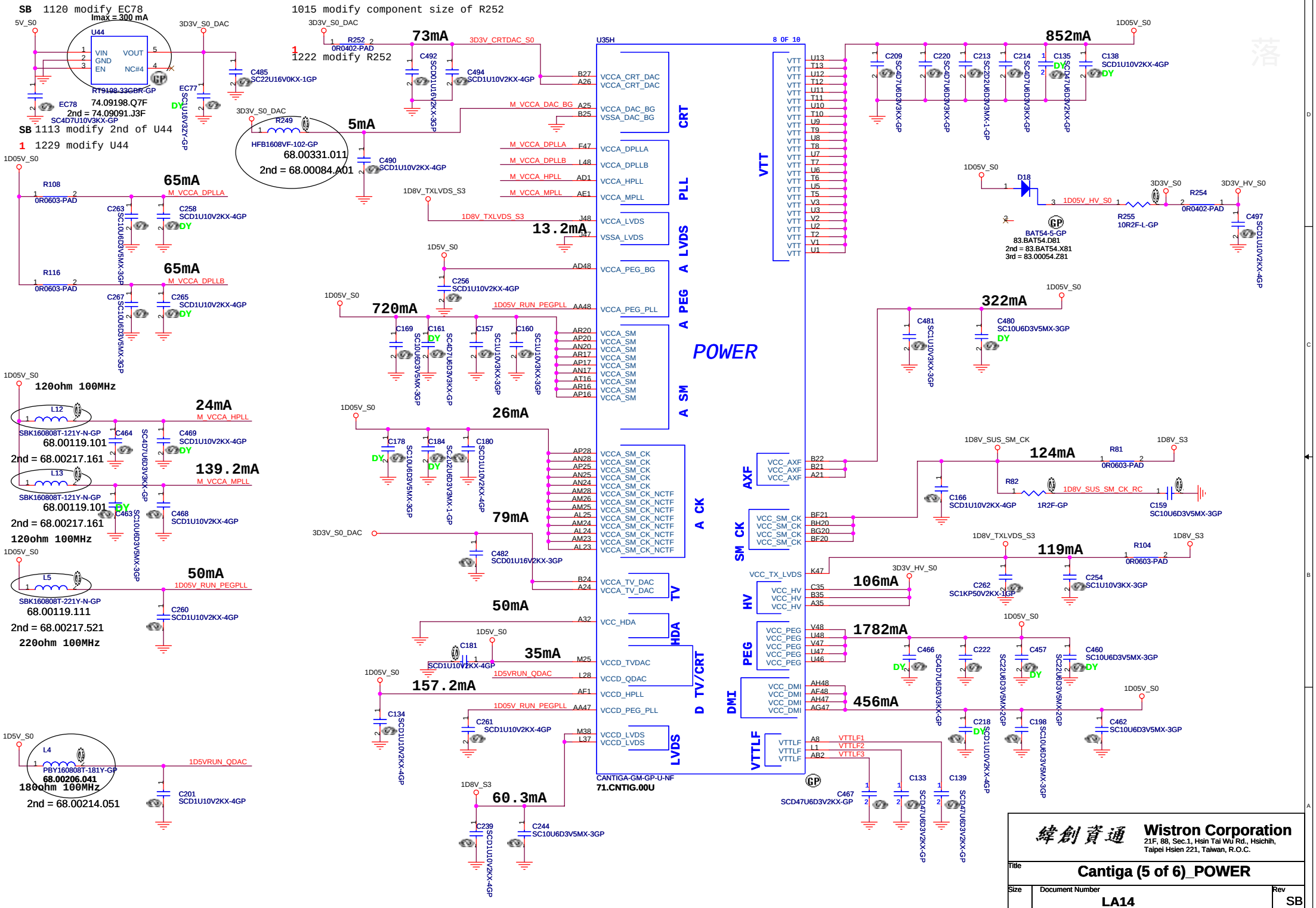
SB 1120 modify EC78
1015 modify component size of R252
1222 modify R252
SB 1113 modify 2nd of U44
1229 modify U44
U44
Imax = 300 mA
RT9198-33GBR-GP
74.09198.Q7F
2nd = 74.09091.J3F
SC4D7U10V3KX-GP
HFB1608VF-102-GP
68.00331.011
2nd = 68.00084.A01
73mA
5mA
65mA
65mA
720mA
13.2mA
26mA
79mA
50mA
35mA
157.2mA
60.3mA
852mA
322mA
124mA
119mA
106mA
1782mA
456mA
24mA
139.2mA
50mA
120ohm 100MHz
68.00119.101
2nd = 68.00217.161
68.00119.111
2nd = 68.00217.521
220ohm 100MHz
68.00206.041
2nd = 68.00214.051
U35H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
BAT54-5-GP
83.BAT54.D81
2nd = 83.BAT54.X81
3rd = 83.00054.Z81
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Title
Cantiga (5 of 6)_POWER
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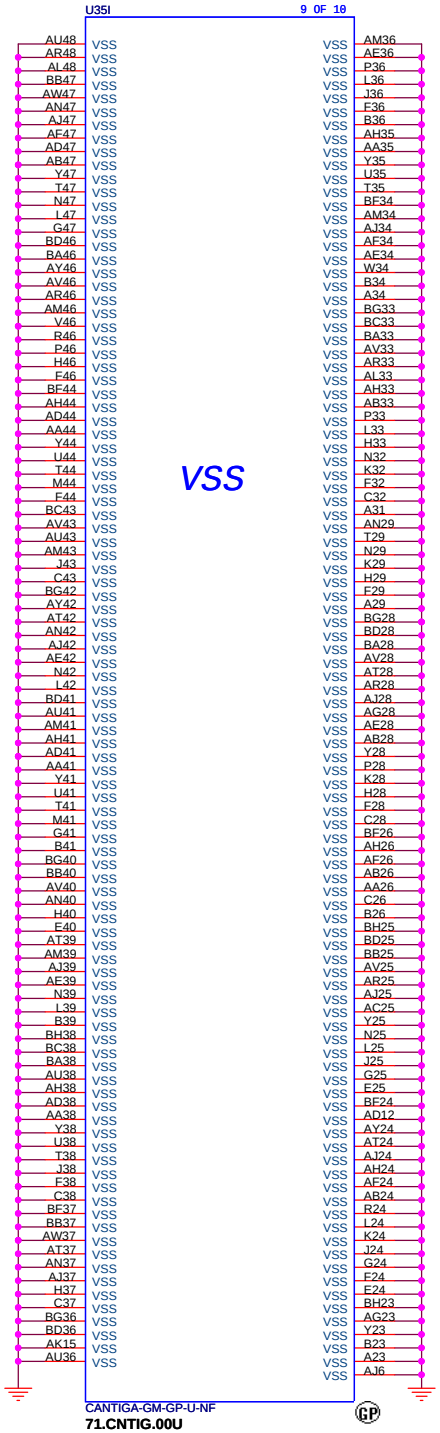

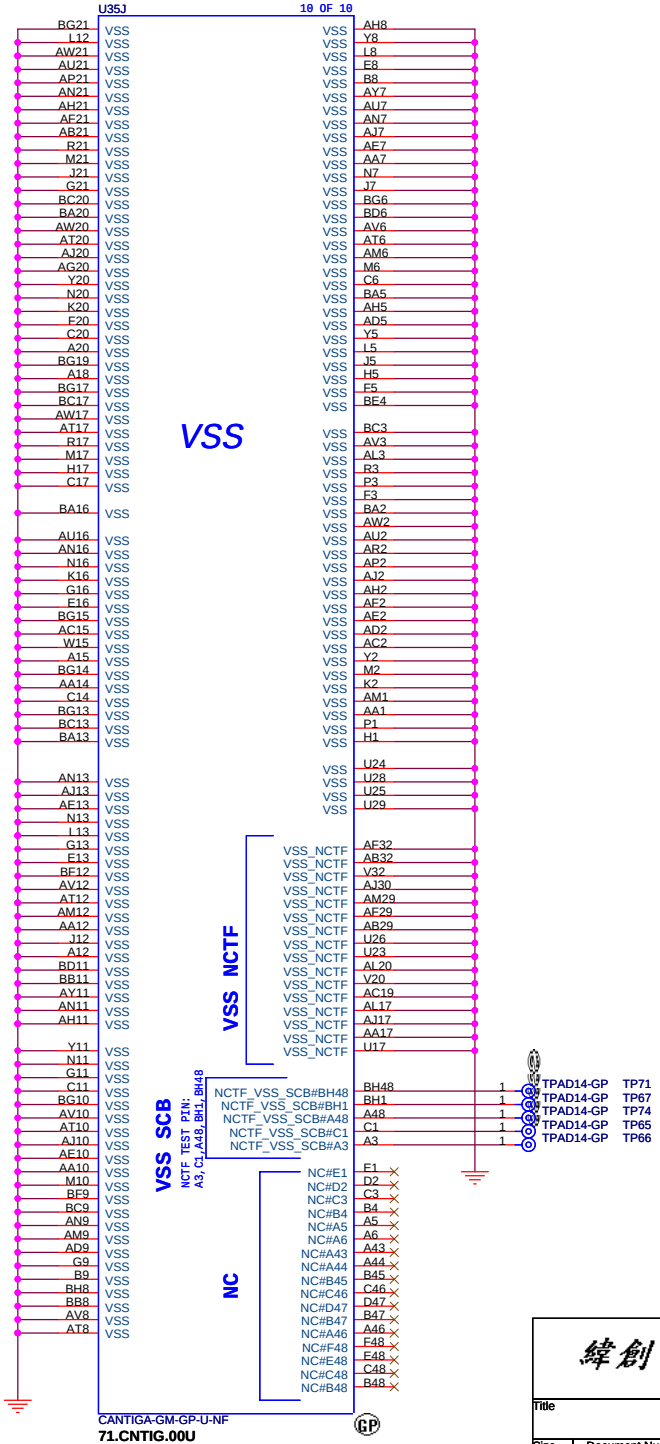

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Title	**Cantiga (6 of 6)**
Size	Document Number: **LA14** — Rev: SB
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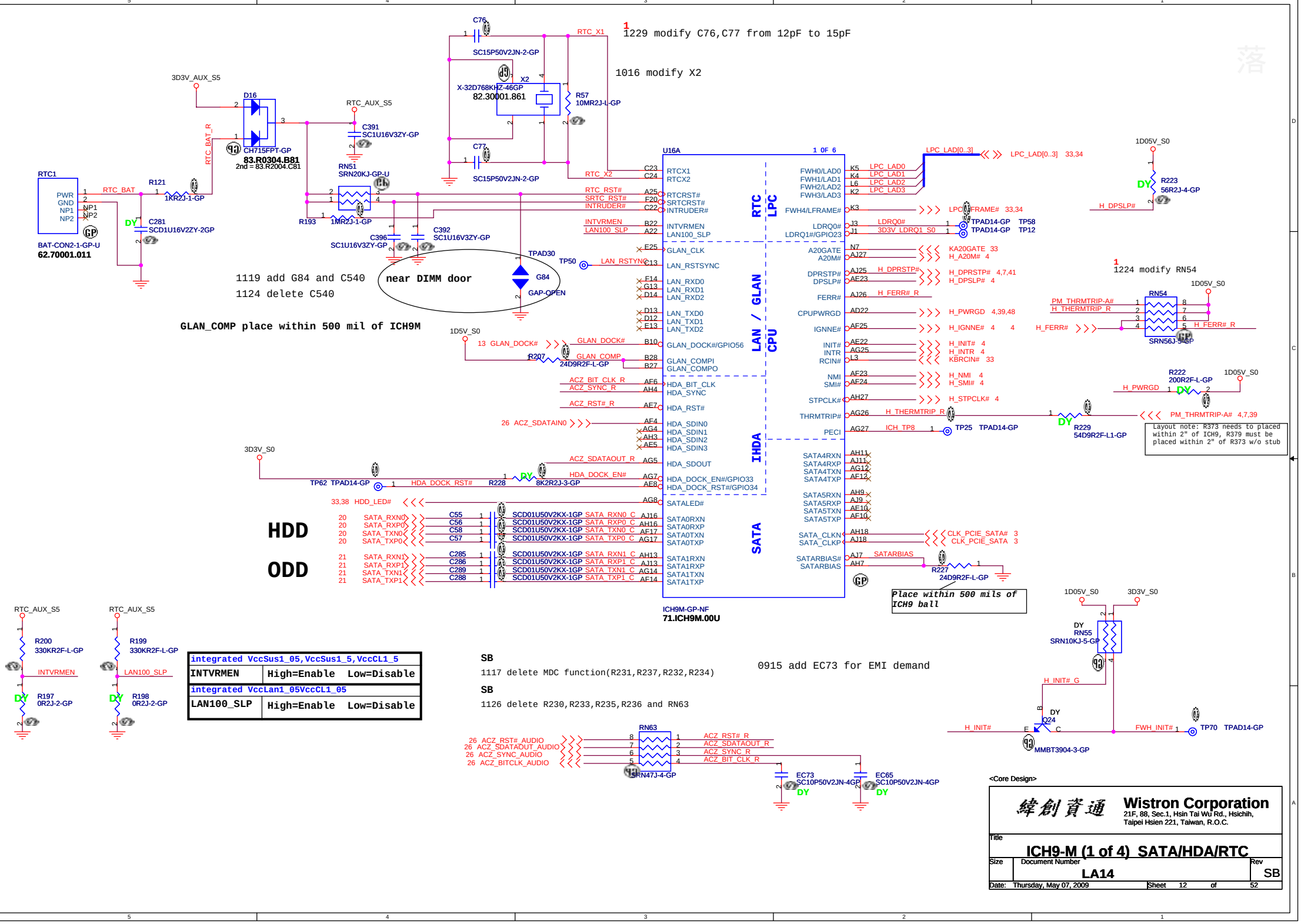
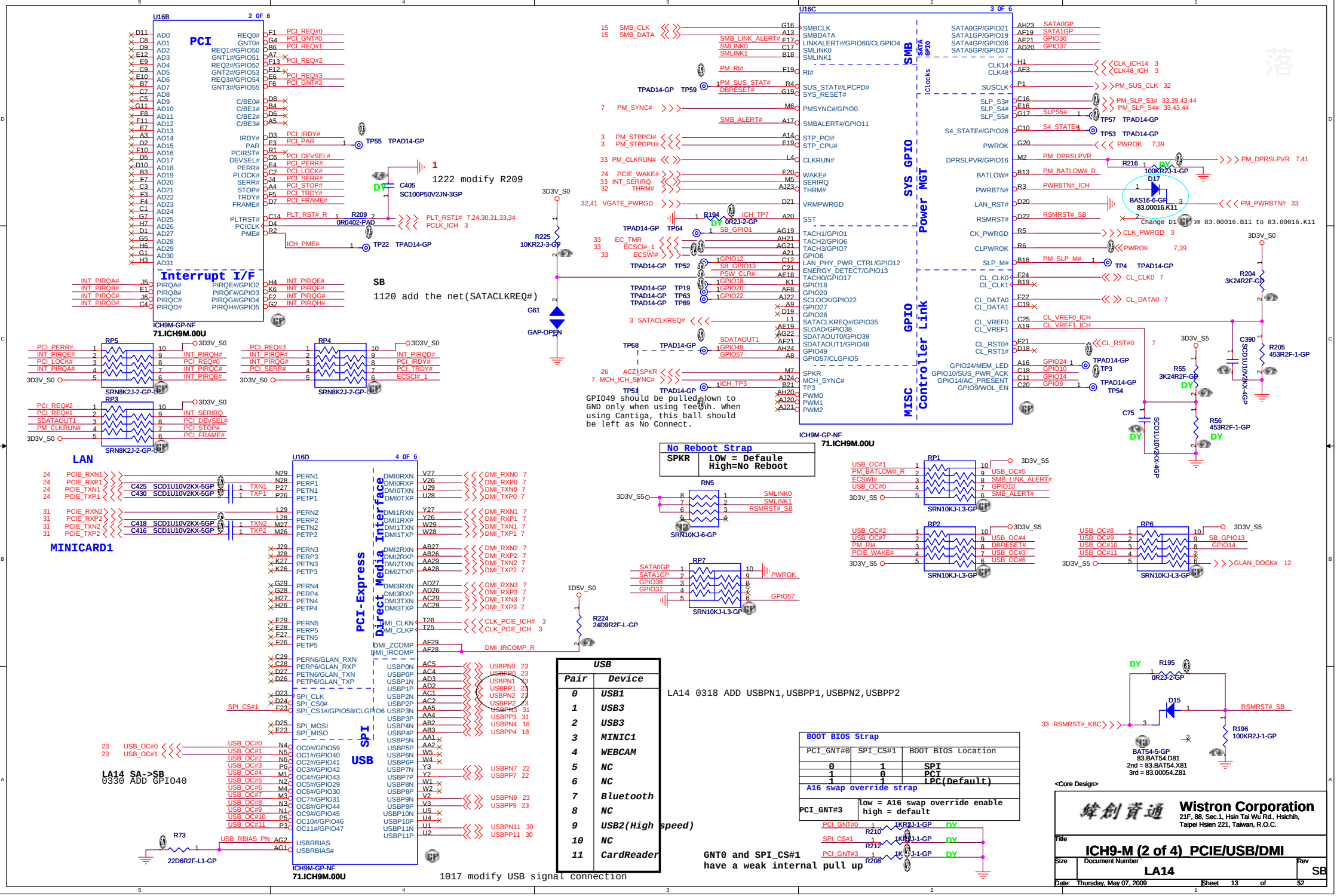

1229 modify C76,C77 from 12pF to 15pF
1016 modify X2
1119 add G84 and C540
1124 delete C540
near DIMM door
GLAN_COMP place within 500 mil of ICH9M
1224 modify RN54
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
Place within 500 mils of ICH9 ball
HDD
ODD
SB
1117 delete MDC function(R231,R237,R232,R234)
SB
1126 delete R230,R233,R235,R236 and RN63
0915 add EC73 for EMI demand
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
U16A
1 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
RTC1
BAT-CONN2-1-GP-U
62.70001.011
D16
CH715FPT-GP
83.R0304.B81
2nd = 83.R2004.C81
X2
X-32D768KHZ-46GP
82.30001.861
RN51
SRN20KJ-GP-U
RN54
SRN56J-5-GP
RN63
SRN47J-4-GP
RN55
SRN10KJ-5-GP
Q24
MMBT3904-3-GP
G84
GAP-OPEN
TPAD30
TP50
TP58
TP12
TP25
TP62
TP70
TPAD14-GP
R57
10MR2J-L-GP
R223
56R2J-4-GP
R222
200R2F-L-GP
R229
54D9R2F-L1-GP
R227
24D9R2F-L-GP
R207
24D9R2F-L-GP
R228
8K2R2J-3-GP
R197
0R2J-2-GP
R198
0R2J-2-GP
R200
330KR2F-L-GP
R199
330KR2F-L-GP
EC73
SC10P50V2JN-4GP
EC65
SC10P50V2JN-4GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4) SATA/HDA/RTC
Size
Document Number
LA14
Rev
SB
Date: Thursday, May 07, 2009
Sheet 12 of 52

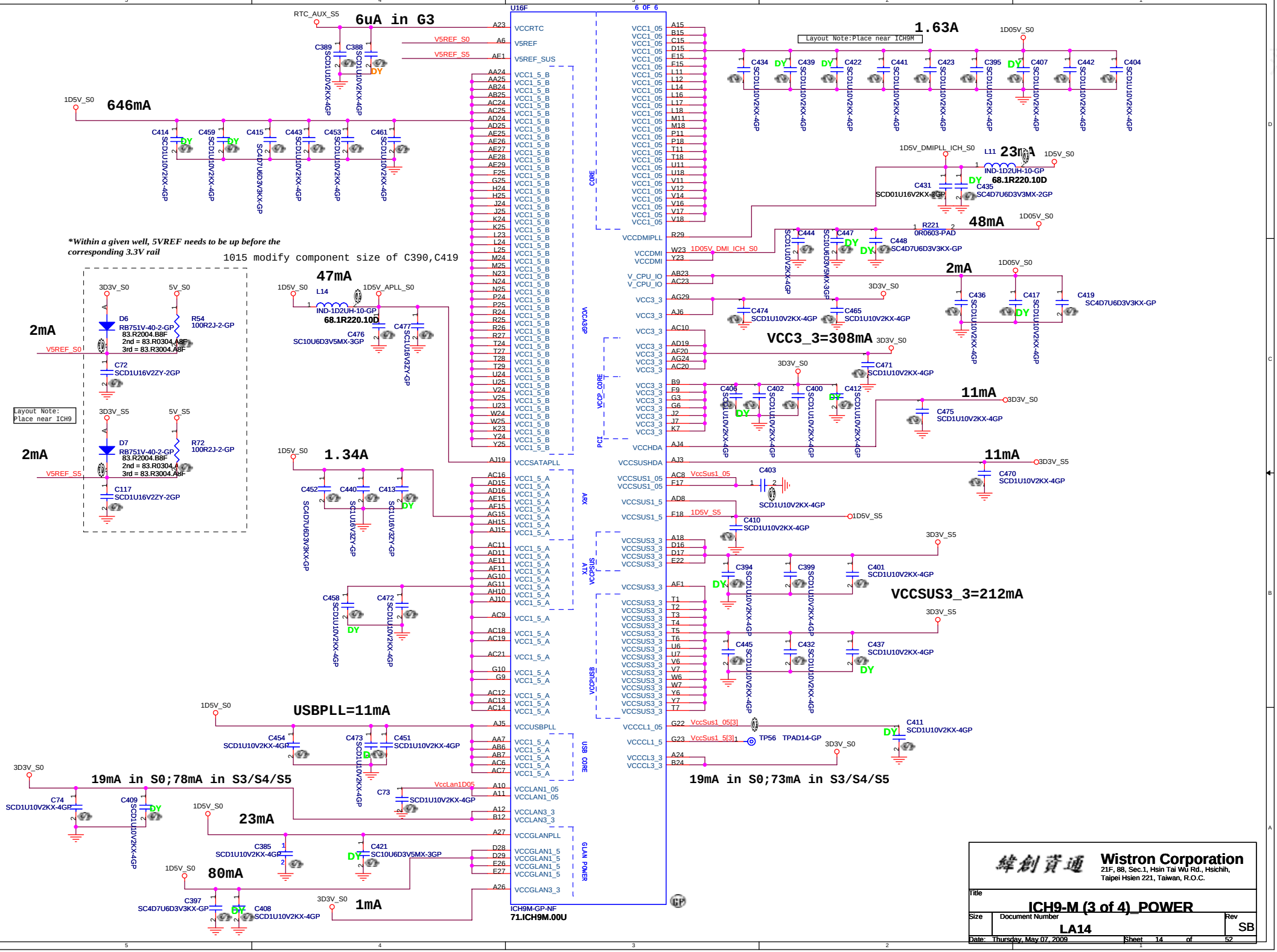


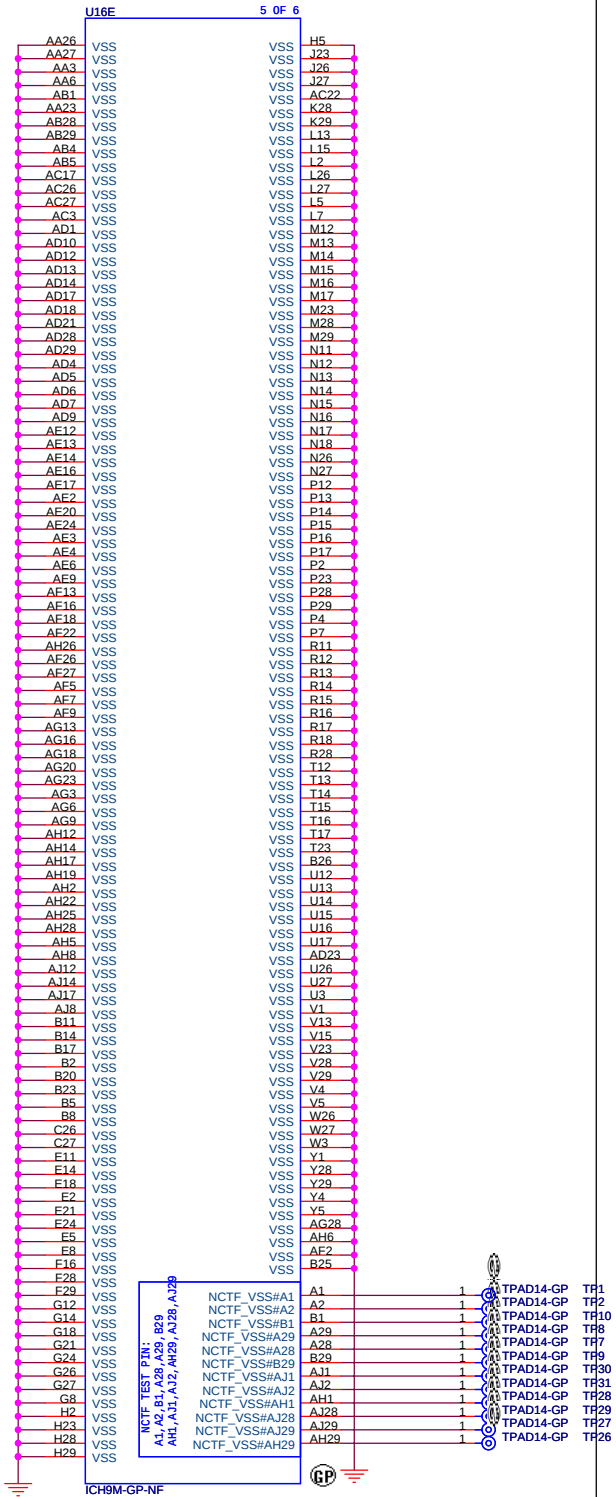
No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

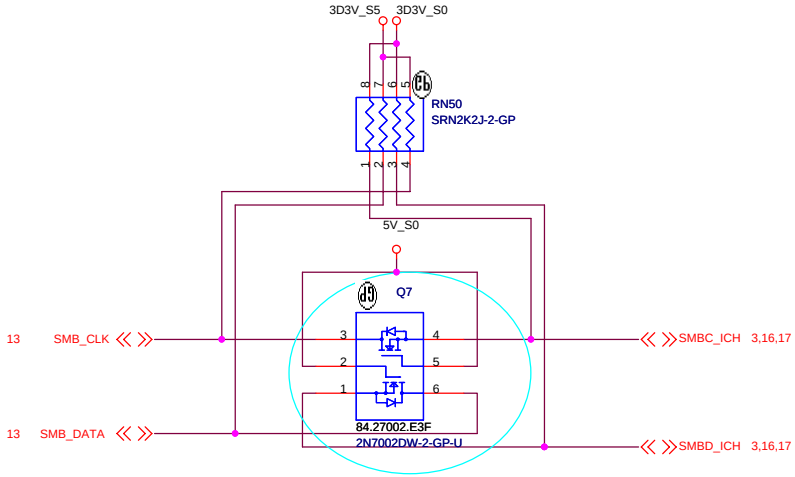
USB	
Pair	Device
0	USB1
1	USB3
2	USB3
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB2(High speed)
10	NC
11	CardReader

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default


6uA in G3
646mA
1.63A
23mA
48mA
2mA
47mA
1.34A
VCC3_3=308mA
11mA
VCCSUS3_3=212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA in S0;73mA in S3/S4/S5
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1015 modify component size of C390,C419
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
U16F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)_POWER
Size
Document Number
LA14
Rev
SB
Date: Thursday, May 07, 2009
Sheet 14 of 52





SMBUS

LA14 SA->SB
0403 Change Q7 from 84.27002.D3F to 84.27002.E3F

緯創資通 **Wistron Corporation**
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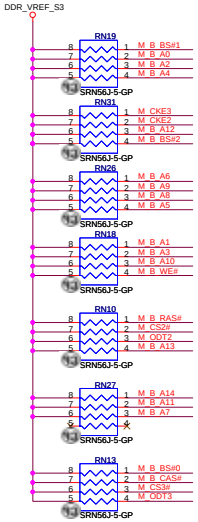
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	ICH9-M (4 of 4)	
Size	Document Number **LA14**	Rev SB
Date: Thursday, May 07, 2009	Sheet 15 of 52	

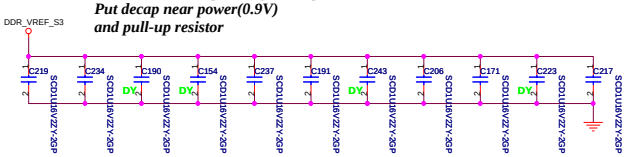
PARALLEL TERMINATION

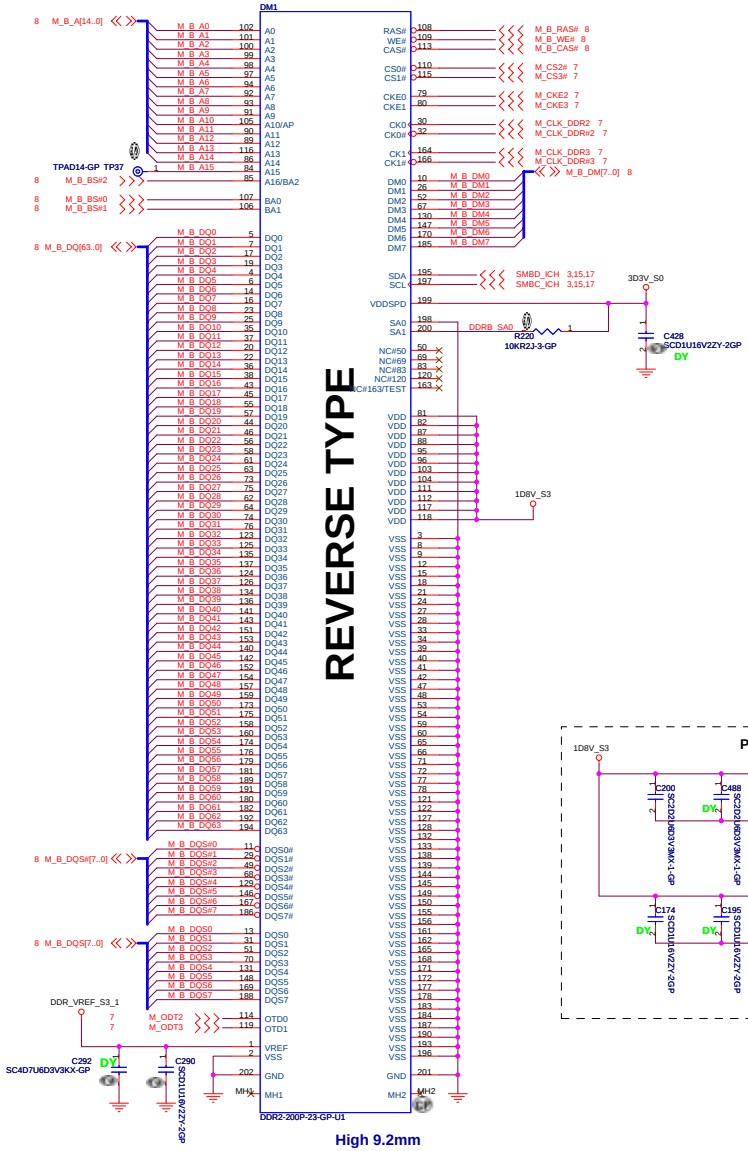
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

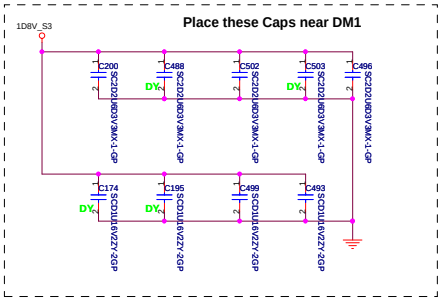
Put decap near power(0.9V) and pull-up resistor





High 9.2mm

62.10017.A71
2nd = 62.10017.B51
3rd = 62.10017.K51



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

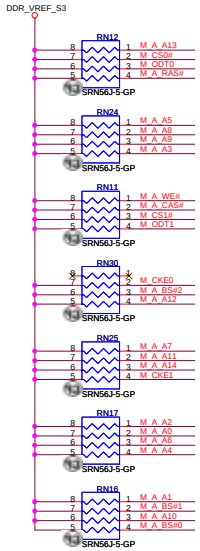
Title: DDR2 Socket 0 (DM1)

Size	Document Number	Rev
	LA14	SB

Date: Thursday, May 07, 2009 Sheet 16 of 52

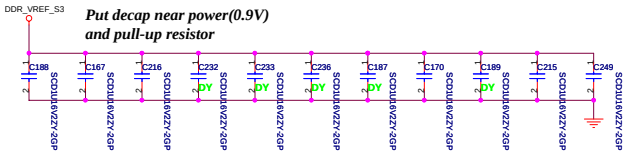
PARALLEL TERMINATION

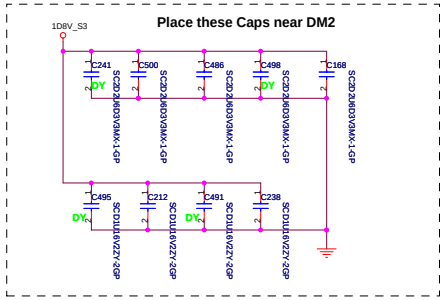
Put decap near power(0.9V) and pull-up resistor

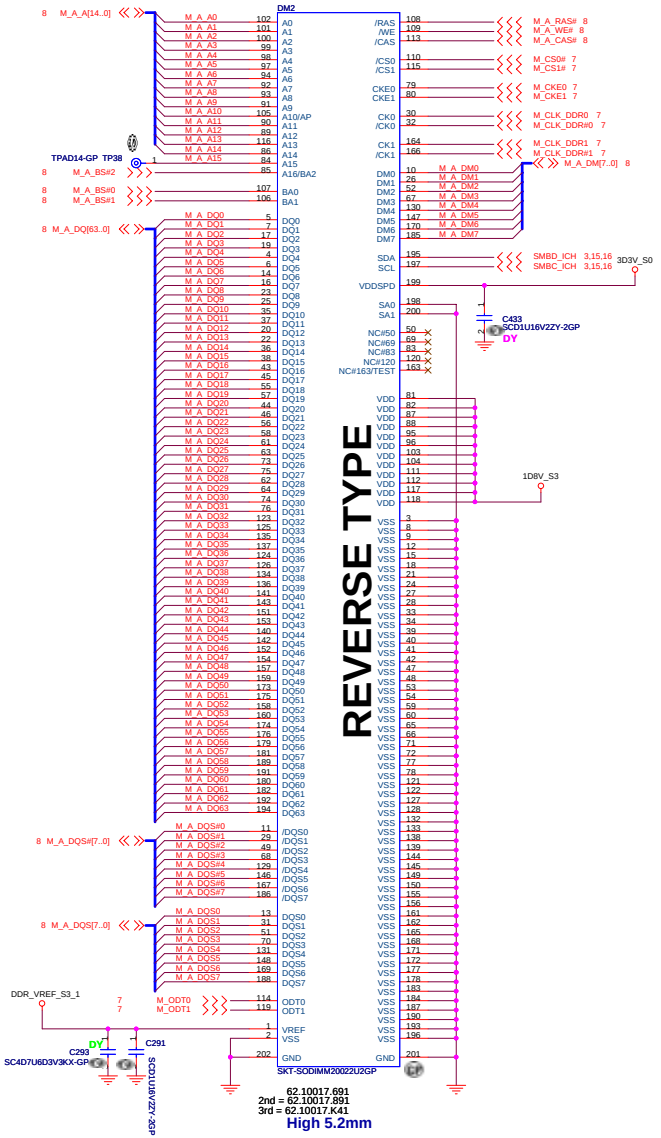


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor





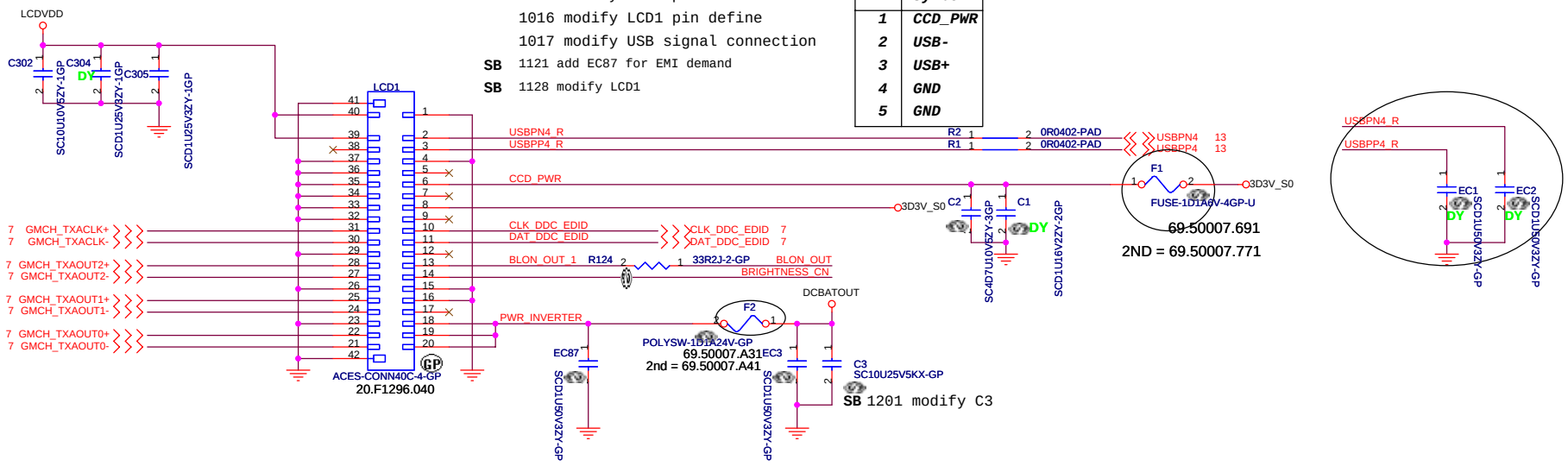


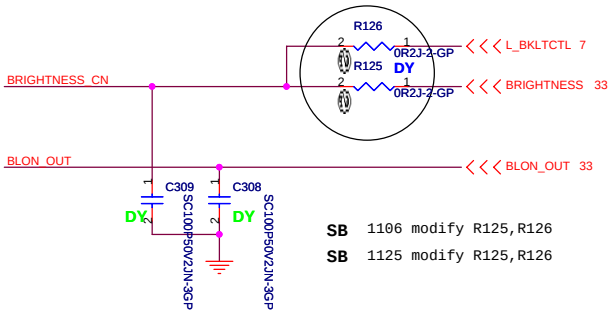
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR2 Socket 1 (DM2)		
Size	Document Number: LA14		Rev: SB
Date: Thursday, May 07, 2009	Sheet 17 of 52		

LCD/CCD CONN

1015 modify F1
1015 modify LCD1 pin define
1016 modify LCD1 pin define
1017 modify USB signal connection
SB 1121 add EC87 for EMI demand
SB 1128 modify LCD1

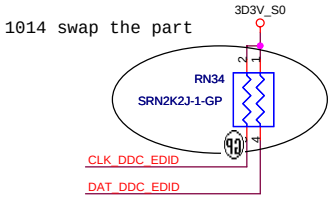
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



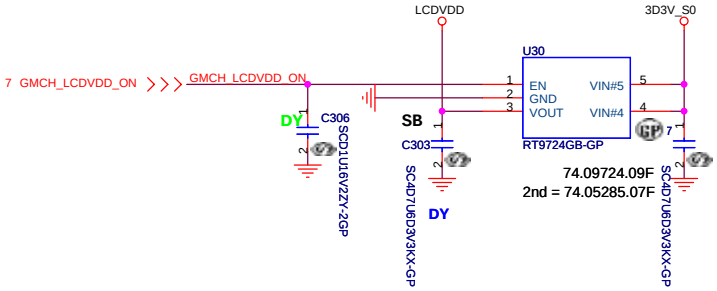


SB 1106 modify R125,R126
SB 1125 modify R125,R126

1014 swap the part



Layout 40 mil



1015 modify component size of C303,C307
1
1229 modify U30

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD CONN		
Size	Document Number	Rev
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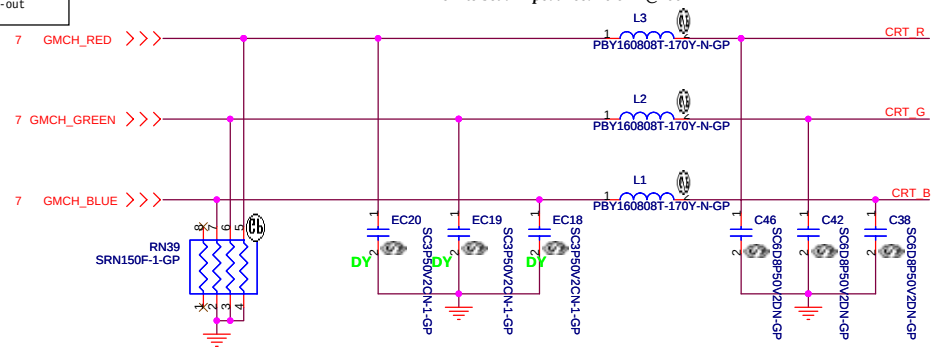
Date: Thursday, May 07, 2009	Sheet 18 of 52	

Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz

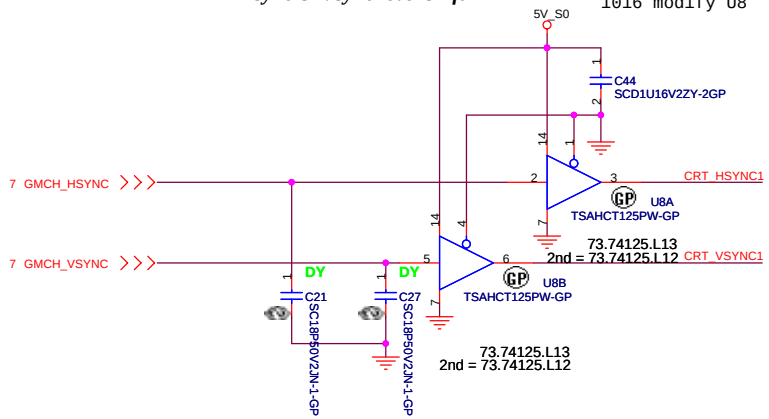


1016 modify L1,L2 and L3
10105 modify L1,L2 and L3

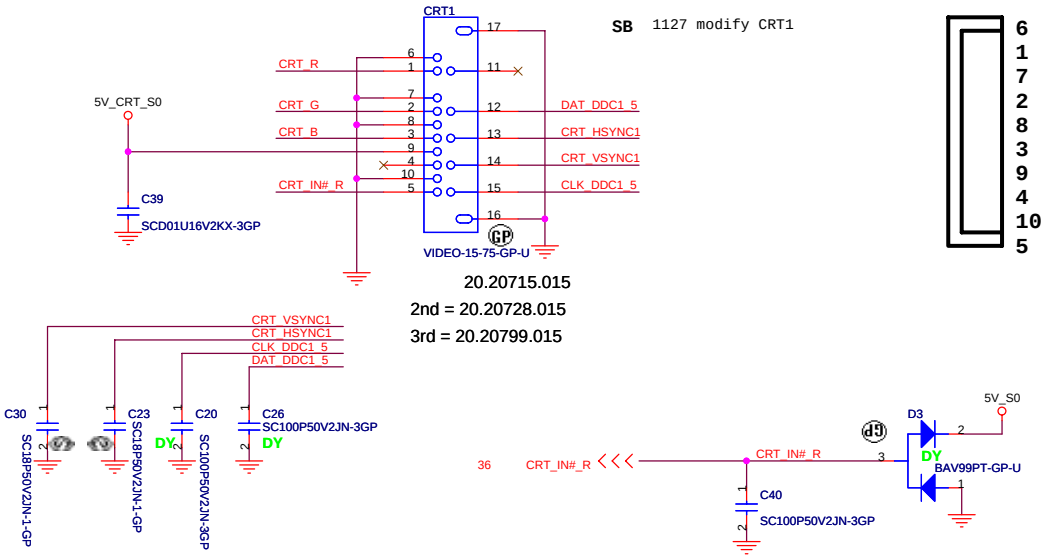
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

1016 modify U8



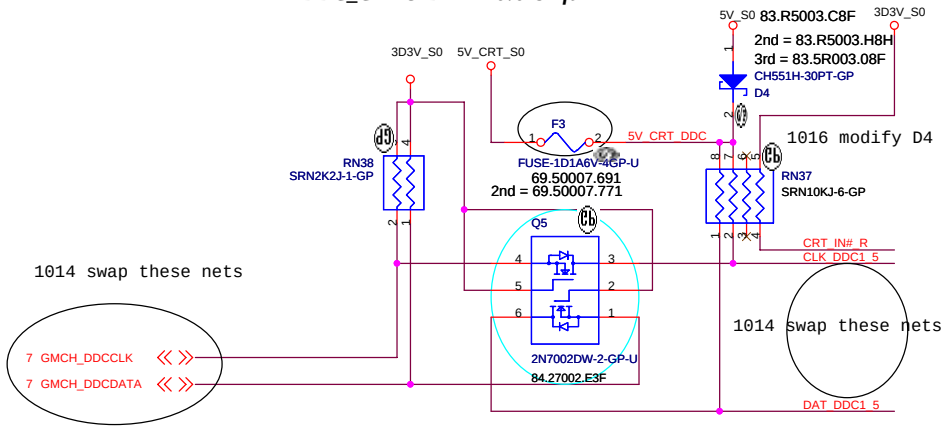
CRT I/F & CONNECTOR



SB 1127 modify CRT1

20.20715.015
2nd = 20.20728.015
3rd = 20.20799.015

DDC_CLK & DATA level shift



1016 modify D4

1014 swap these nets

1014 swap these nets

LA14 SA->SB
0403 Change Q5 from 84.27002.D3F to 84.27002.E3F

<Core Design>

緯創資通 **Wistron Corporation**
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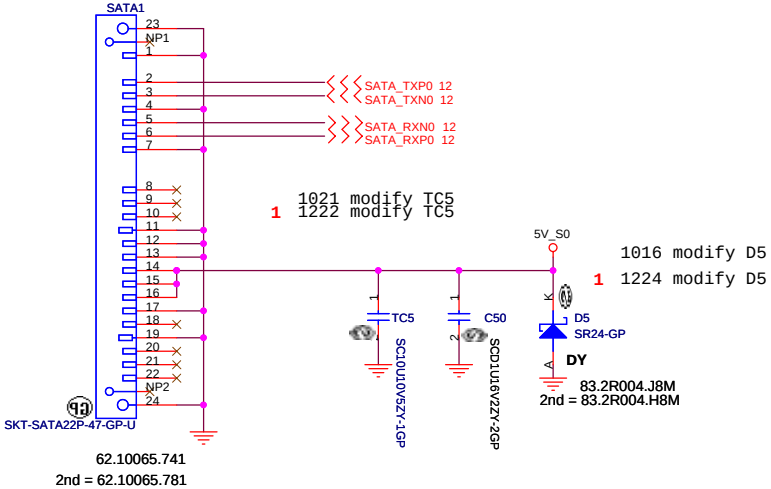
Title		
CRT Connector		
Size	Document Number	Rev
	LA14	SB
Date: Thursday, May 07, 2009	Sheet 19 of 52	

SATA Connector

0912 add these parts for EMI demand
1001 delete these parts for EMI demand
1021 modify SATA1



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDD**	
Size	Document Number **LA14**	Rev SB
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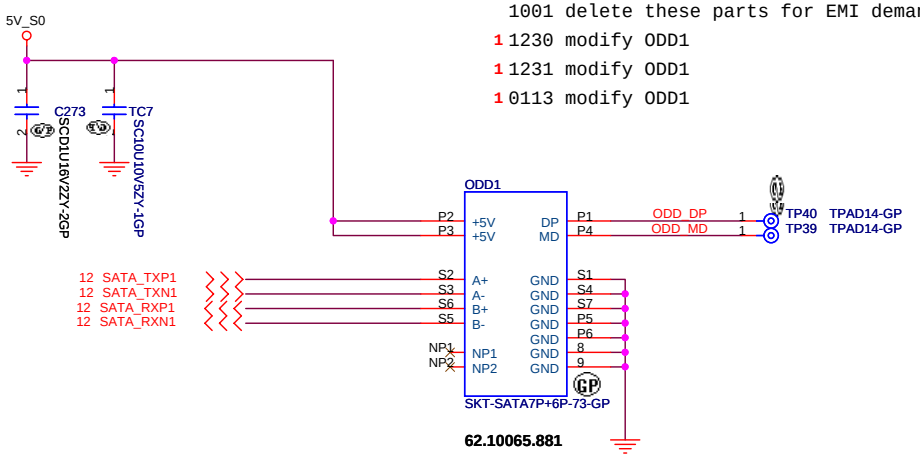
SATA ODD Connector

```
  0912 add these parts for EMI demand
  1001 delete these parts for EMI demand
1 1230 modify ODD1
1 1231 modify ODD1
1 0113 modify ODD1
```



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ODD**
Size / Document Number	**LA14**
Rev	SB
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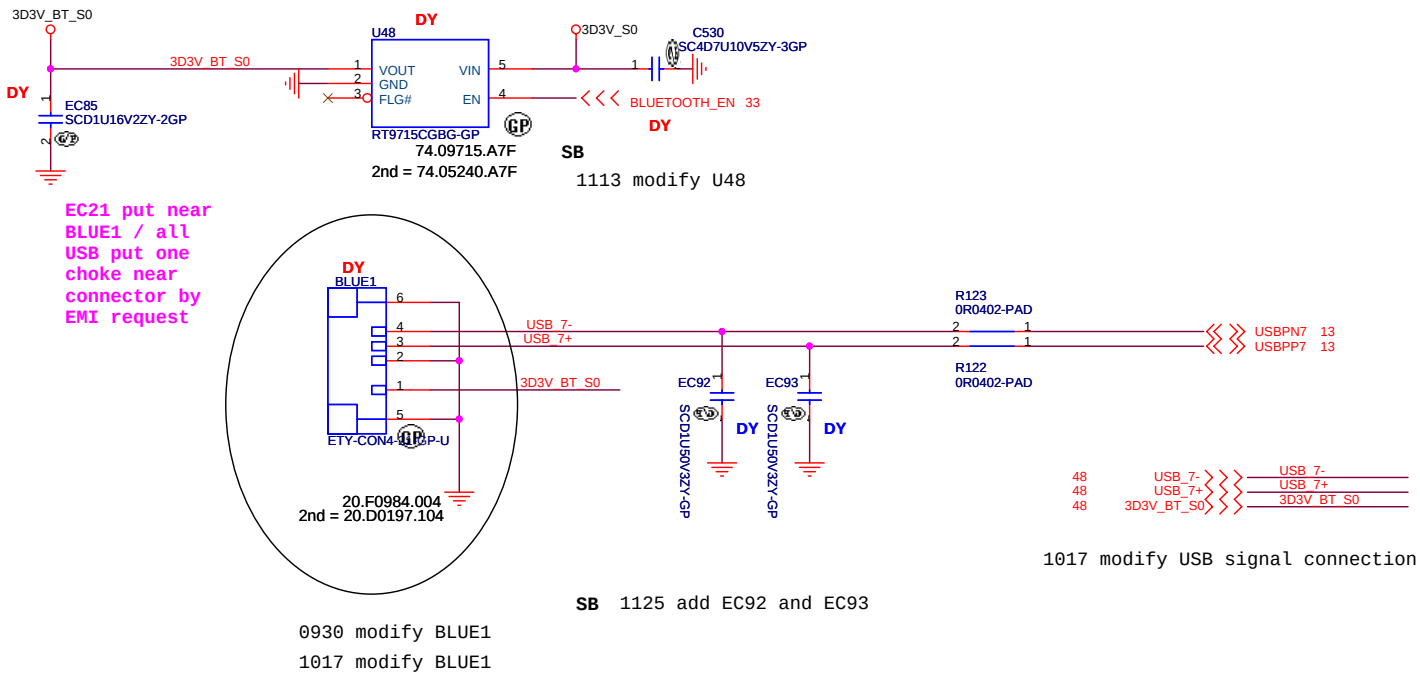
BLUETOOTH MODULE

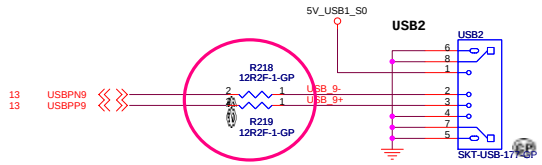
1.5A / High Active Voltage 2V



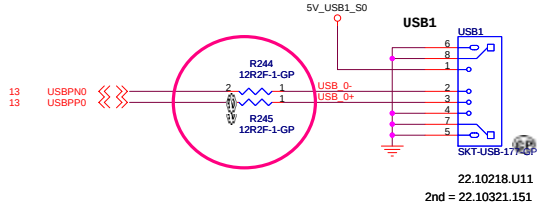
<Core Design>

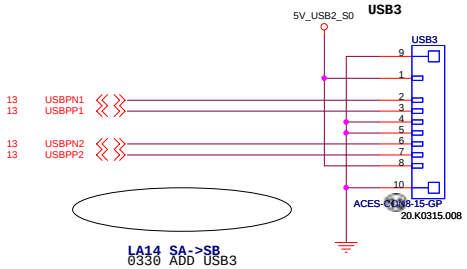
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Bluetooth**	
Size	Document Number **LA14**	Rev SB
Date: Thursday, May 07, 2009	Sheet 22 of 52	

1017 modify USB signal connection
1021 modify and swap these parts(USB1 and USB2)



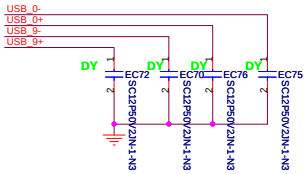
Modify 04/27 Change R218,R219,R244,R245 from 0ohm to 12ohm

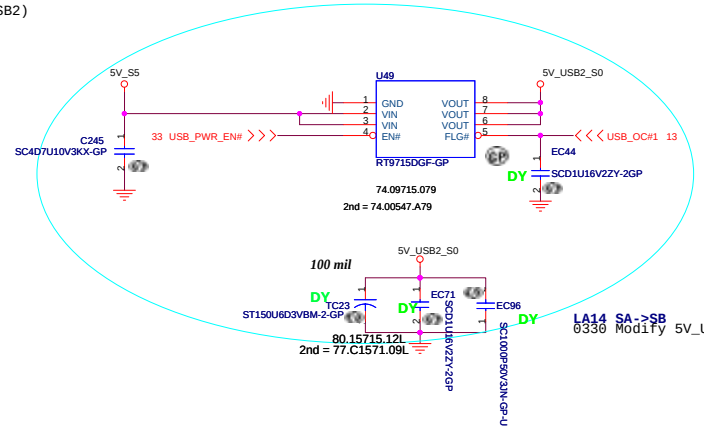




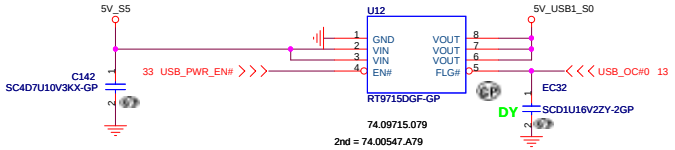
LA14 SA->SB
0330 ADD USB3

0912 add these parts for EMI demand



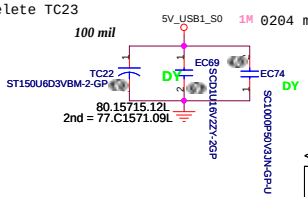


LA14 SA->SB
0330 Modify 5V_USB2_S0,ADD U49 C245,TC23



1021 delete TC23

0204 modify the symbol of EC74 (page23)



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB		
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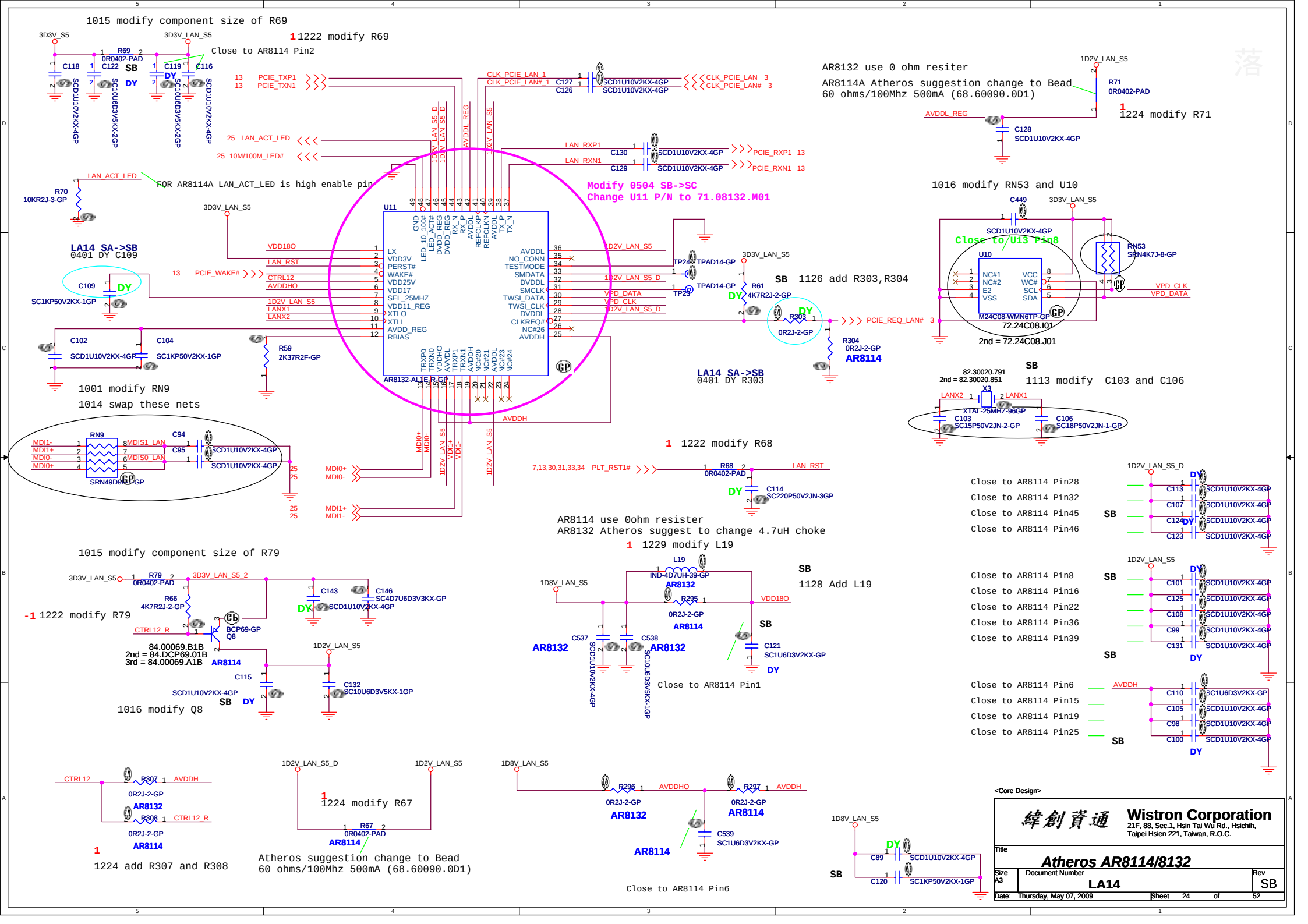
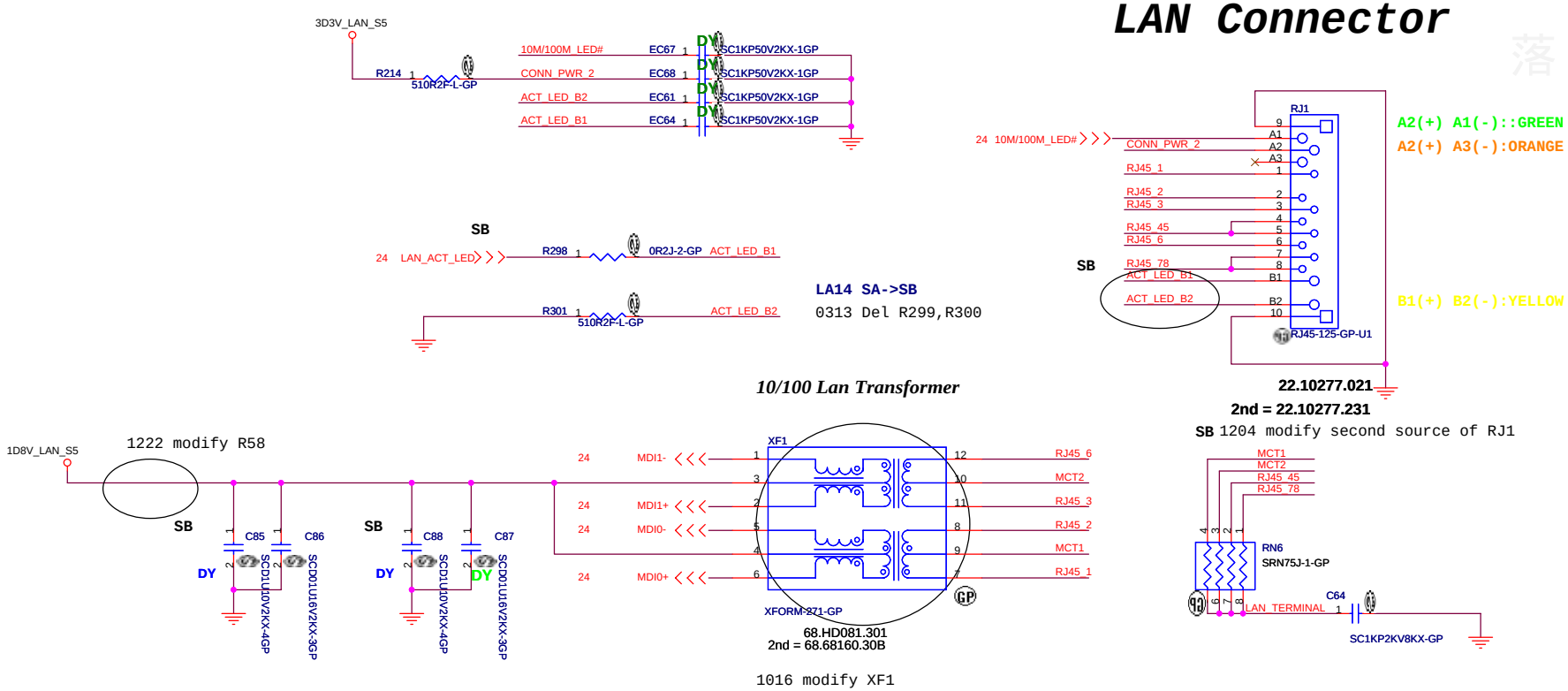

1015 modify component size of R69
1 1222 modify R69
Close to AR8114 Pin2
AR8132 use 0 ohm resiter
AR8114A Atheros suggestion change to Bead
60 ohms/100Mhz 500mA (68.60090.0D1)
1 1224 modify R71
FOR AR8114A LAN_ACT_LED is high enable pin
Modify 0504 SB->SC
Change U11 P/N to 71.08132.M01
1016 modify RN53 and U10
Close to U13 Pin8
LA14 SA->SB
0401 DY C109
SB 1126 add R303,R304
LA14 SA->SB
0401 DY R303
1001 modify RN9
1014 swap these nets
1 1222 modify R68
1113 modify C103 and C106
AR8114 use 0ohm resister
AR8132 Atheros suggest to change 4.7uH choke
1 1229 modify L19
SB
1128 Add L19
1015 modify component size of R79
-1 1222 modify R79
1016 modify Q8
Close to AR8114 Pin1
1 1224 add R307 and R308
1 1224 modify R67
Atheros suggestion change to Bead
60 ohms/100Mhz 500mA (68.60090.0D1)
Close to AR8114 Pin6
Close to AR8114 Pin28
Close to AR8114 Pin32
Close to AR8114 Pin45
Close to AR8114 Pin46
Close to AR8114 Pin8
Close to AR8114 Pin16
Close to AR8114 Pin22
Close to AR8114 Pin36
Close to AR8114 Pin39
Close to AR8114 Pin6
Close to AR8114 Pin15
Close to AR8114 Pin19
Close to AR8114 Pin25
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Atheros AR8114/8132
Size A3
Document Number
LA14
Rev SB
Date: Thursday, May 07, 2009
Sheet 24 of 52

LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	LA14	SB

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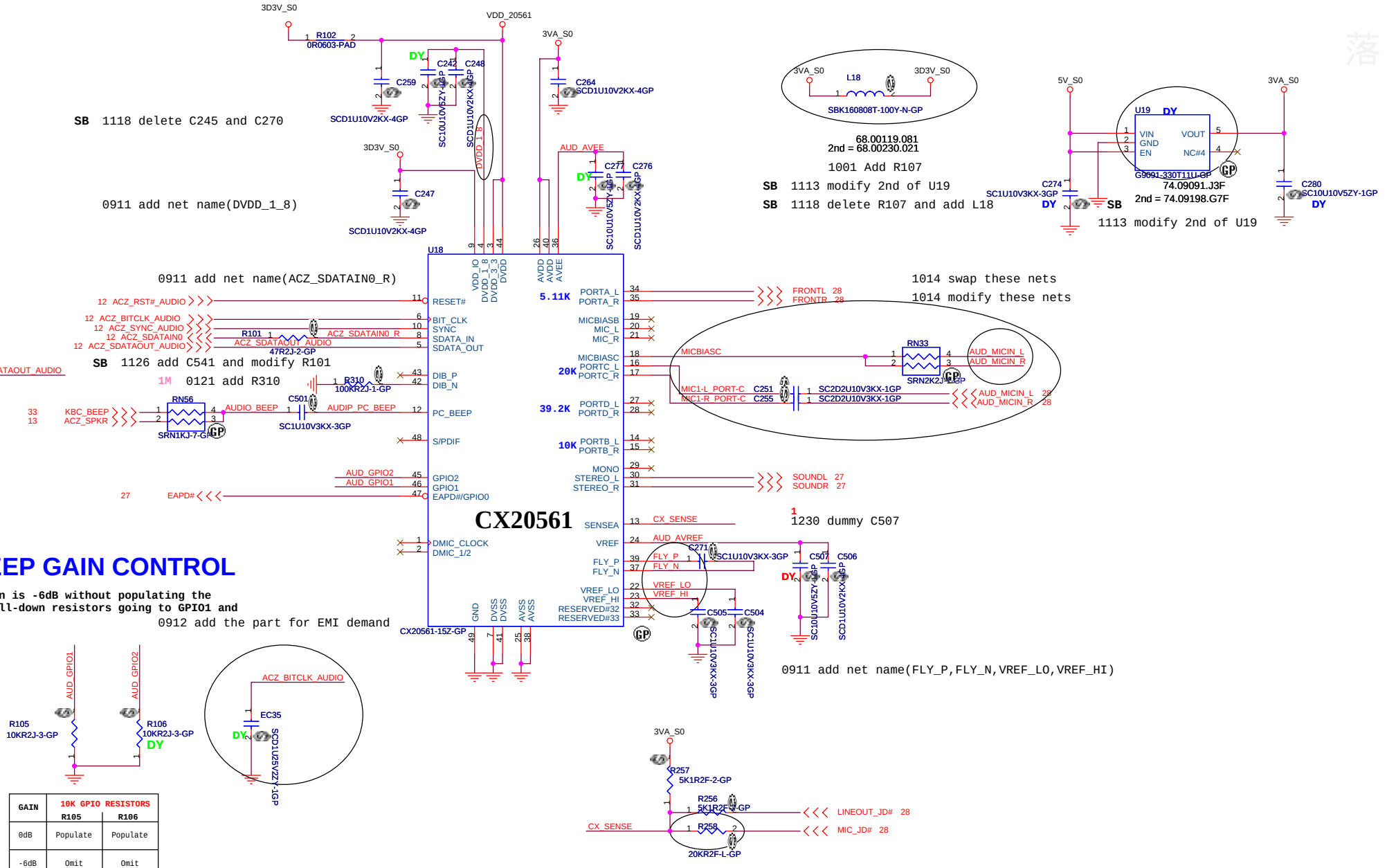

PC BEEP GAIN CONTROL

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

0912 add the part for EMI demand

GAIN	10K GPIO RESISTORS	
	R105	R106
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec CX20561**

Size: A3 | Document Number: LA14 | Rev: SB

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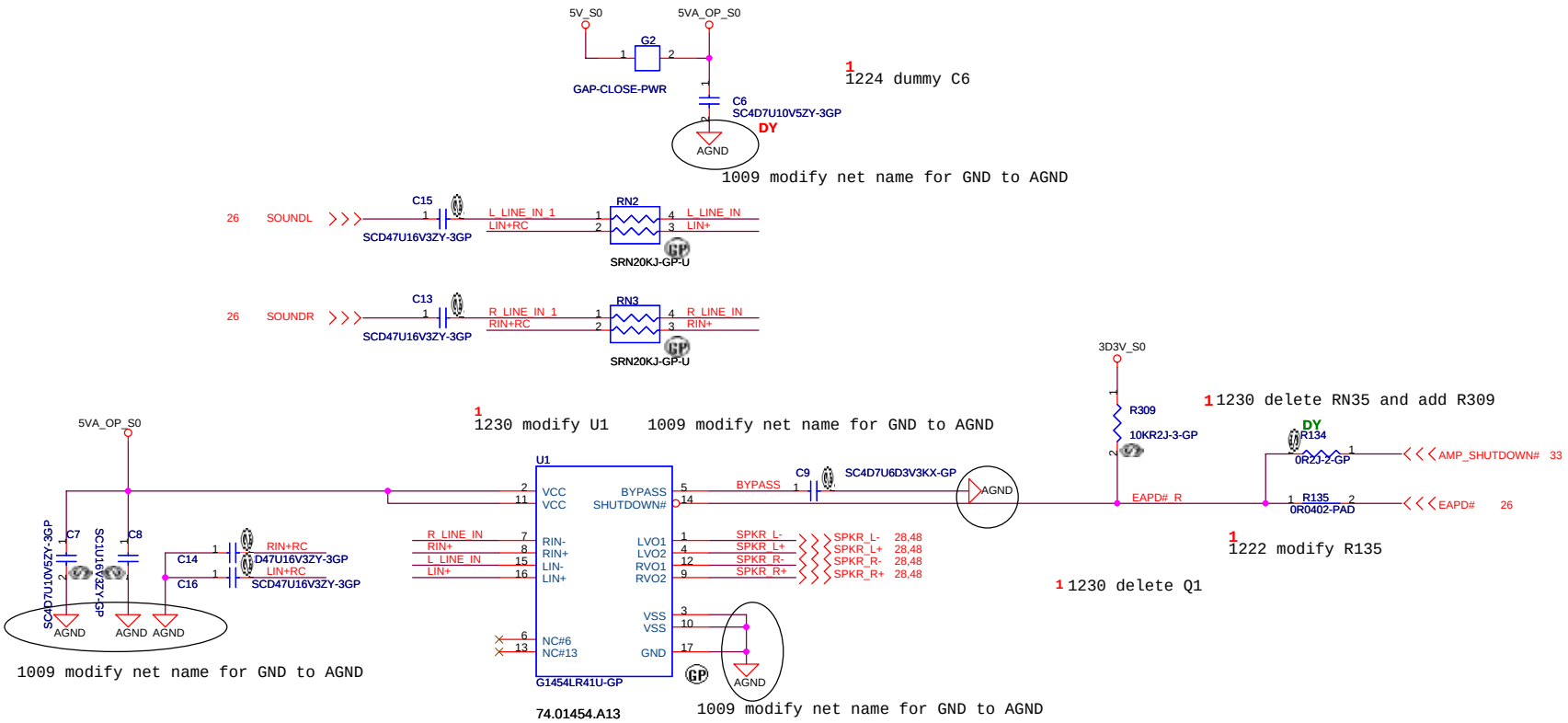
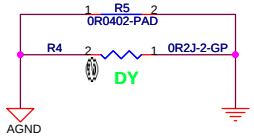
AUDIO OP AMPLIFIER

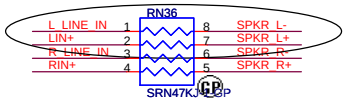


AC decopling

1222 modify R5



1014 swap these nets



SB 1204 modify RN36

落

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

Size | Document Number: LA14 | Rev: SB

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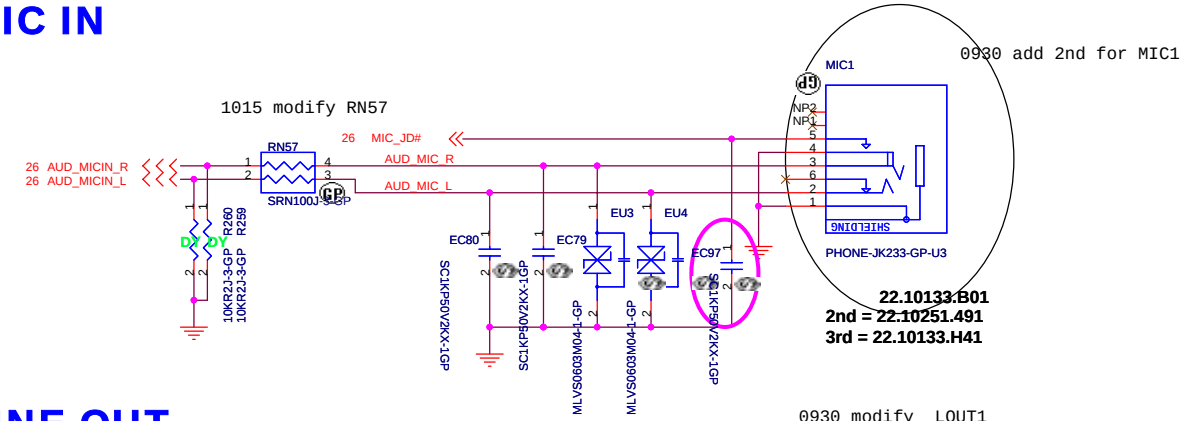
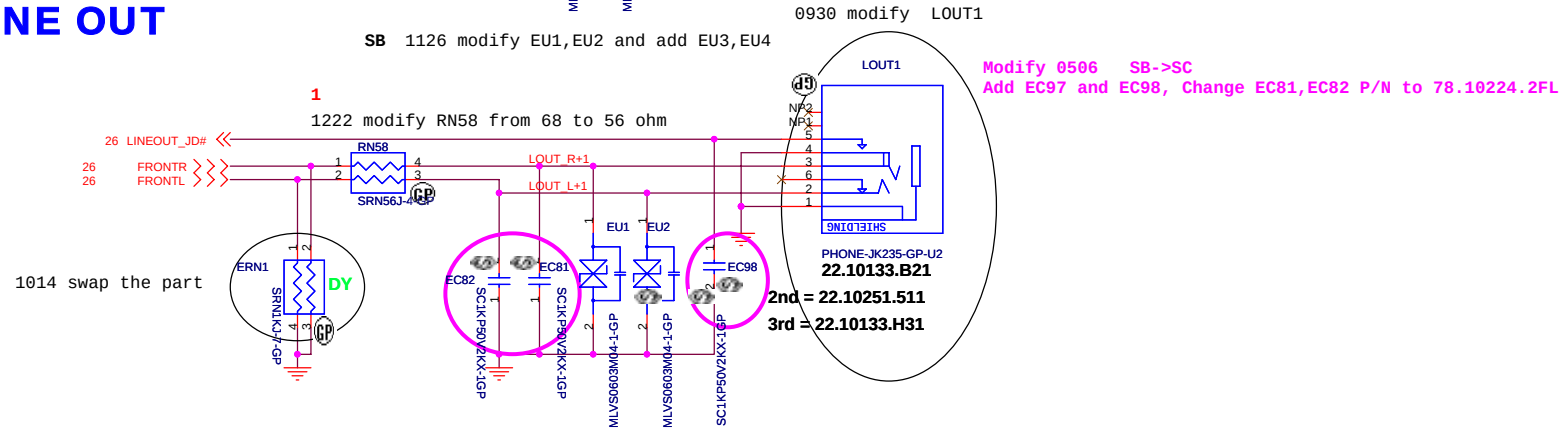
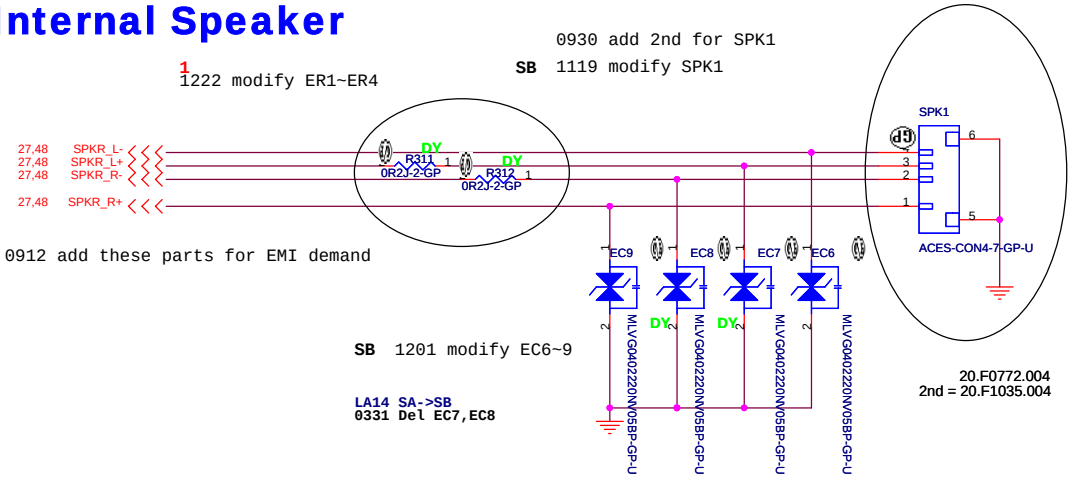
MIC IN



LINE OUT



Internal Speaker



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO JACK	
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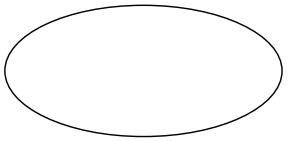
MDC 1.5 CONN

0912 add the part for EMI demand

1002 modify MDC1

SB

1112 delete MDC function



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**MDC**	
Size	Document Number: LA14	Rev: SB
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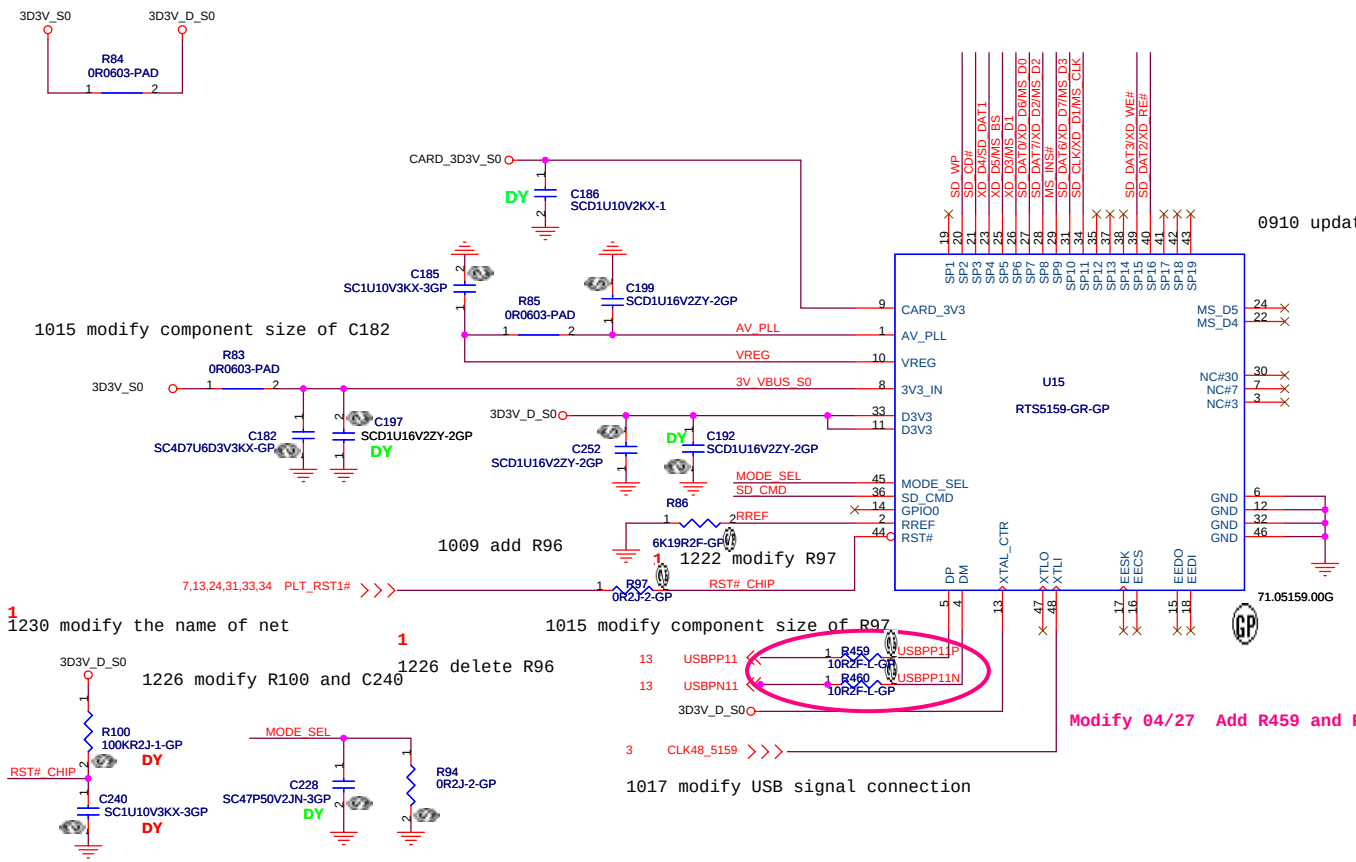


0910 update footprint of U15

1015 modify component size of C182

1009 add R96

1222 modify R97

1230 modify the name of net

1015 modify component size of R97

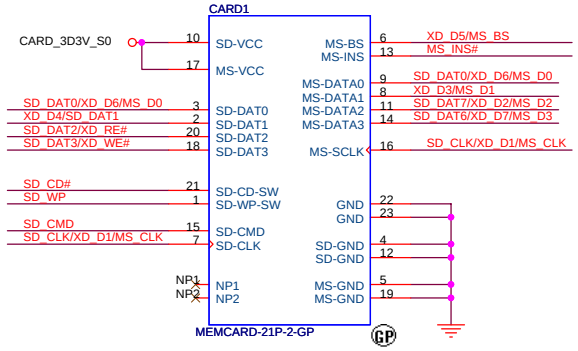
1226 delete R96

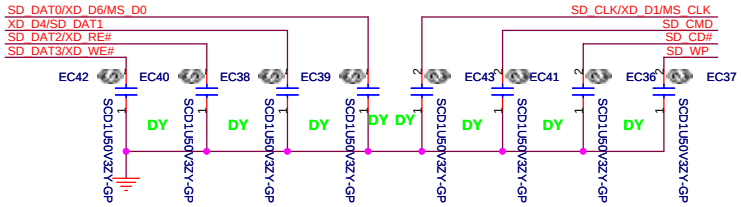
1226 modify R100 and C240

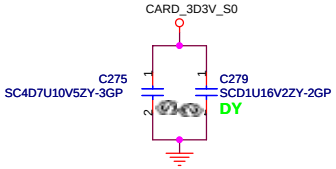
Modify 04/27 Add R459 and R460

1017 modify USB signal connection

3 IN1 CARD-READER (SD/MMC/MS)







1009 modify this net

1013 modify card1

1 1222 modify card1 from 20.I0043.001 to 20.I0043.011

1 1229 modify card1

LA14 SA 0217 modify card1 from 20.I0043.011 to 20.I0033.021

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CARD READER- RTS5159	
Size	Document Number: LA14	Rev: SB
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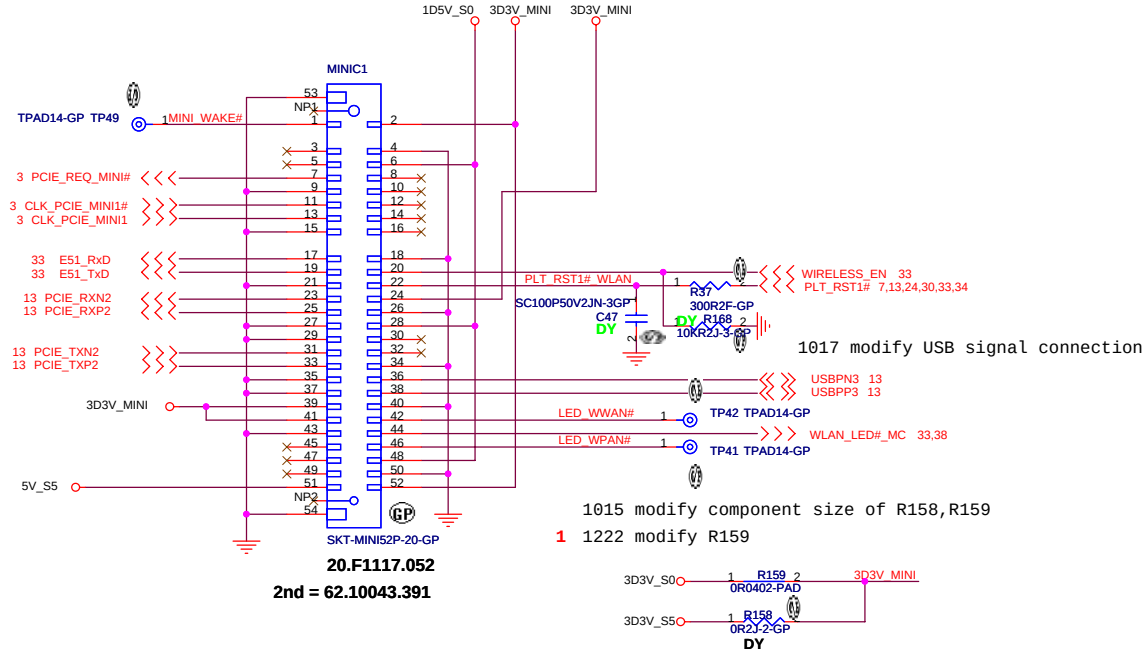
Mini Card Connector(WLAN)



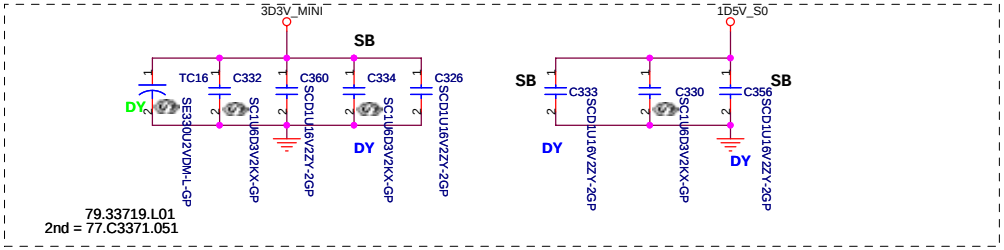
1017 modify USB signal connection

1015 modify component size of R158,R159

1 1222 modify R159

1021 modify TC16

Place near MINIC1



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**MINI CARD**	
Size	Document Number **LA14**	Rev SB
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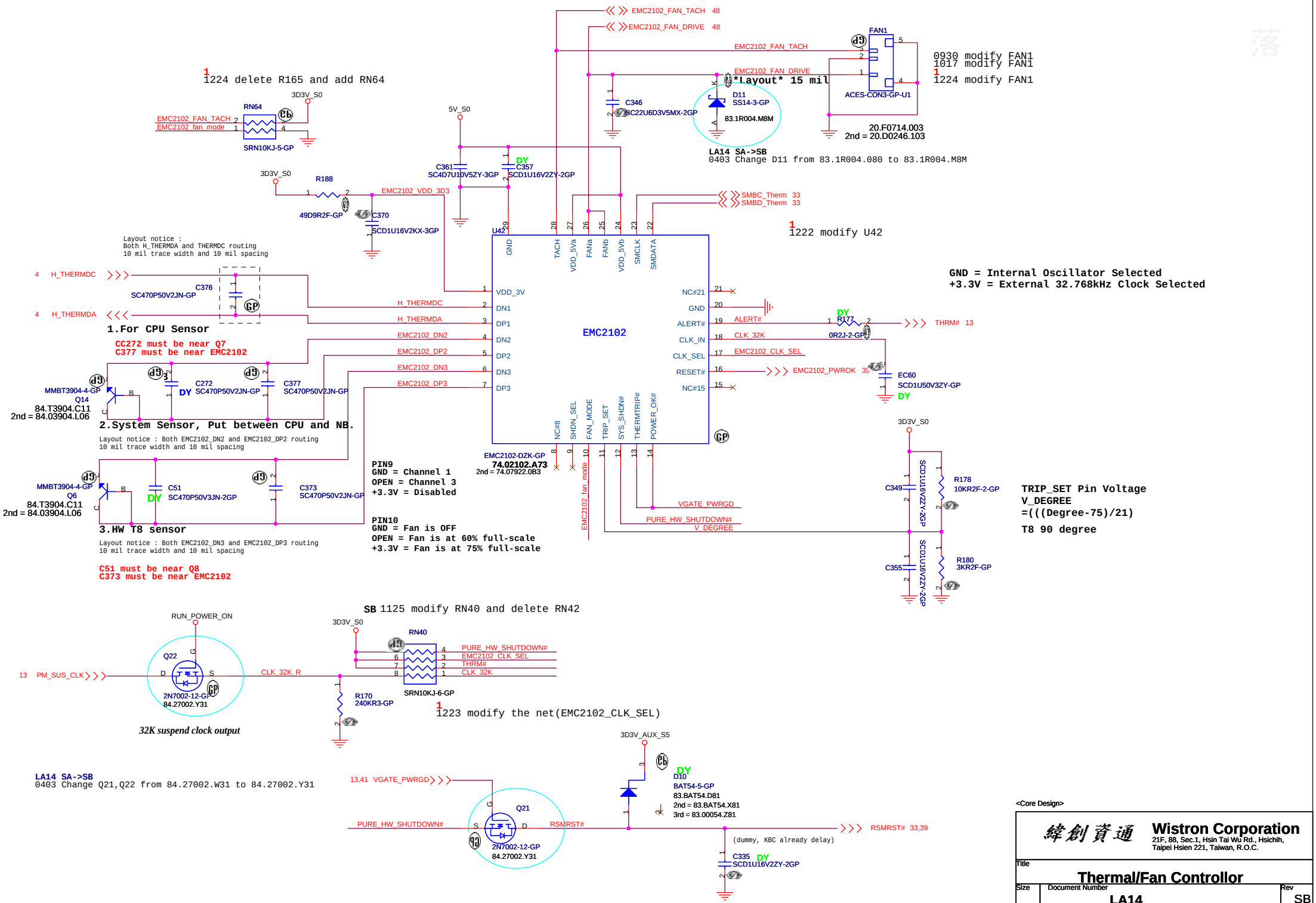

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

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	LA14	SB

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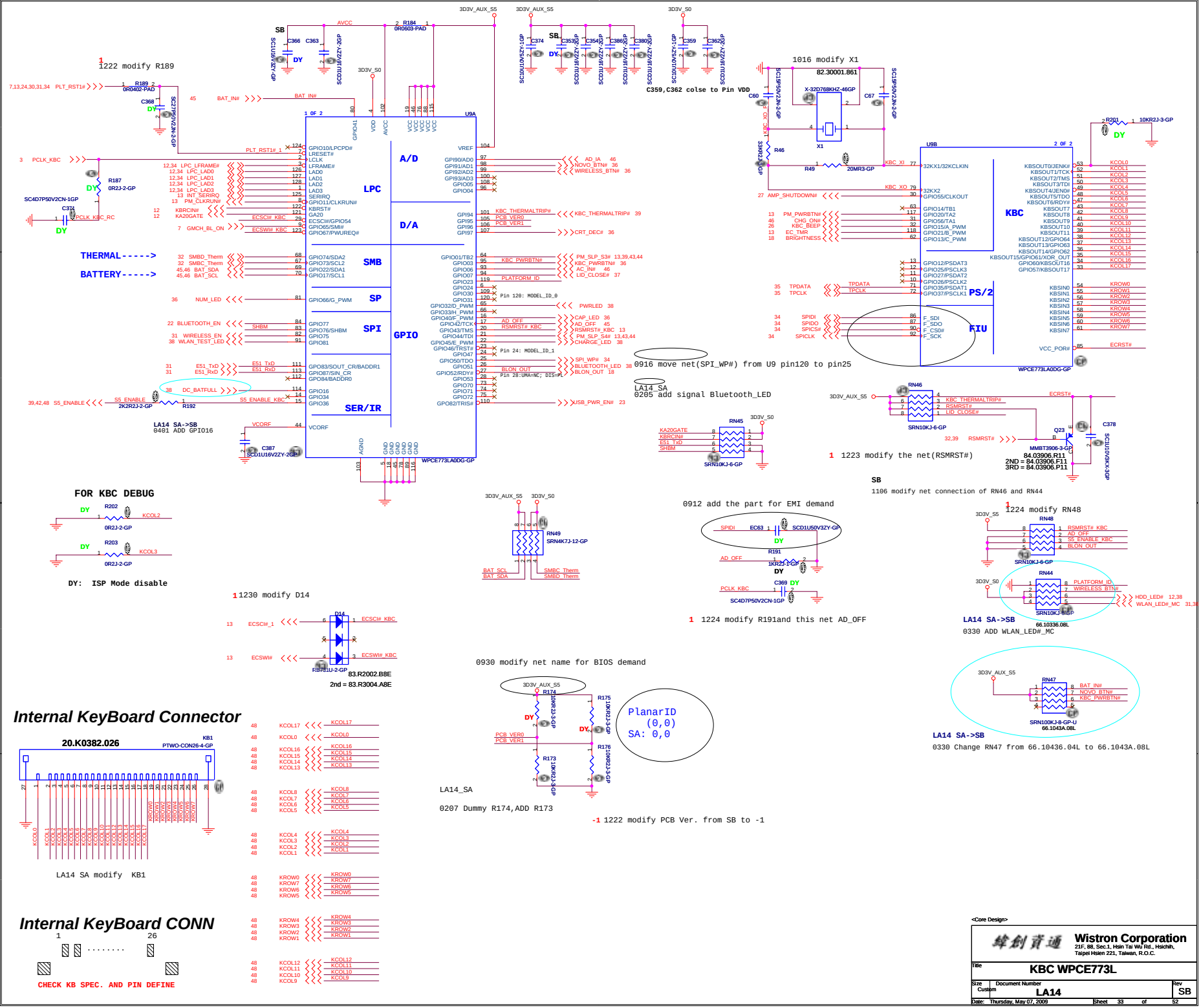
1222 modify R189
1016 modify X1
82.30001.861
C359,C362 colse to Pin VDD
U9A
WPCE773LA0DG-GP
U9B
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
LA14 SA->SB
0401 ADD GPIO16
0916 move net(SPI_WP#) from U9 pin120 to pin25
LA14_SA
0205 add signal Bluetooth_LED
1223 modify the net(RSMRST#)
SB
1106 modify net connection of RN46 and RN44
FOR KBC DEBUG
DY: ISP Mode disable
0912 add the part for EMI demand
1224 modify R191and this net AD_OFF
1224 modify RN48
LA14 SA->SB
0330 ADD WLAN_LED#_MC
1230 modify D14
83.R2002.B8E
2nd = 83.R3004.A8E
0930 modify net name for BIOS demand
PlanarID
(0,0)
SA: 0,0
LA14_SA
0207 Dummy R174,ADD R173
-1 1222 modify PCB Ver. from SB to -1
LA14 SA->SB
0330 Change RN47 from 66.10436.04L to 66.1043A.08L
Internal KeyBoard Connector
20.K0382.026
LA14 SA modify KB1
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPCE773L
LA14
SB
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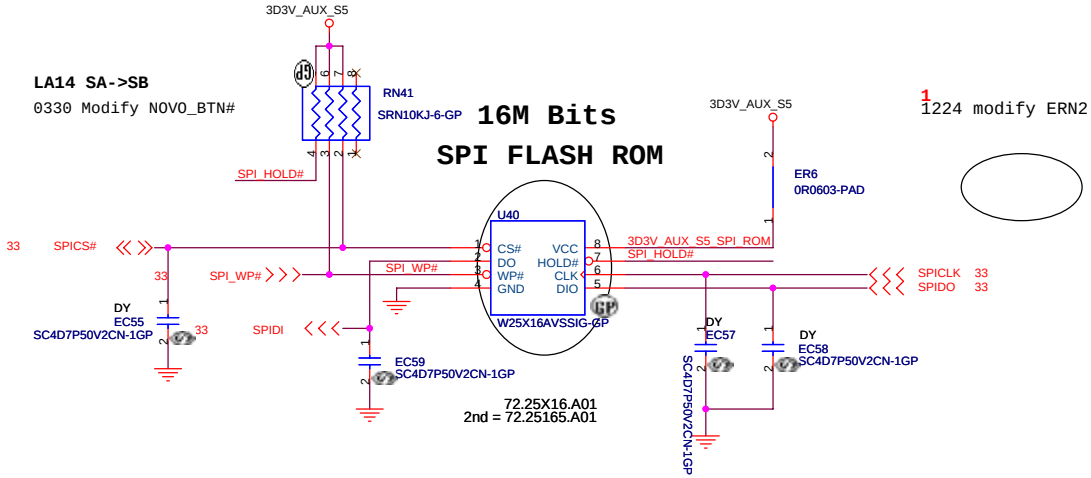
LA14 SA->SB

0330 Modify NOVO_BTN#

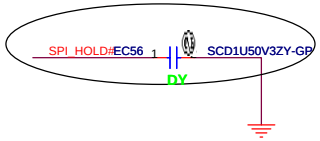


1

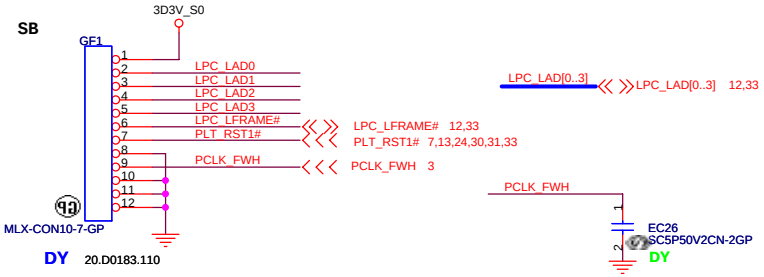
1224 modify ERN2

1013 modify U40 from 72.25X16.001 to 72.25X16.A01

0912 add the part for EMI demand



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BIOS/GOLDEN FINGER	
Size	Document Number LA14	Rev SB
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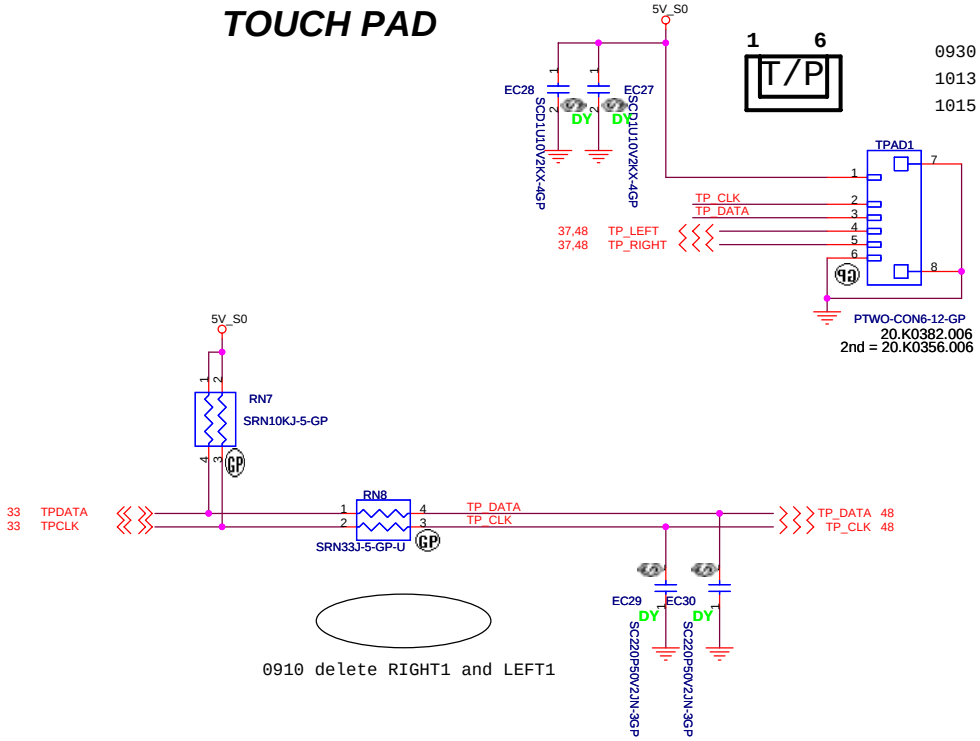
TOUCH PAD



0930 modify TPAD1 1124 modify TPAD1
1013 modify TPAD1
1015 modify TPAD1

0910 delete RIGHT1 and LEFT1

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Touch pad**	
Size	Document Number **LA14**	Rev SB
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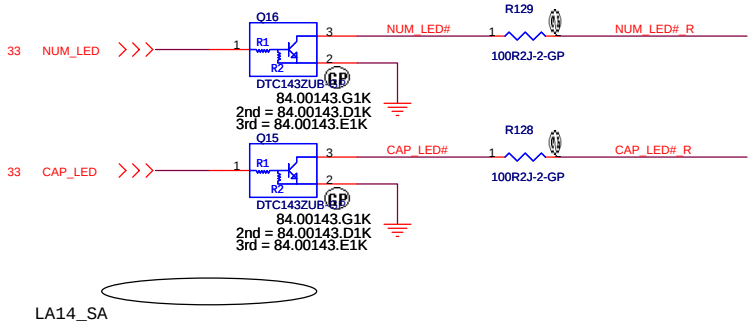
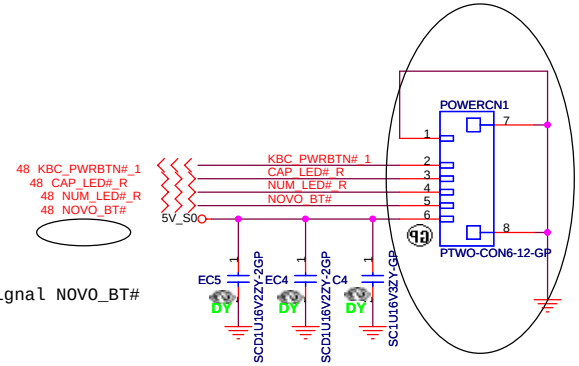


LA14_SA

0205 remove signals(TP_LOCK_LED,TP_LOCK_LED#,TP_LOCK_LED#_R)and R132,Q17



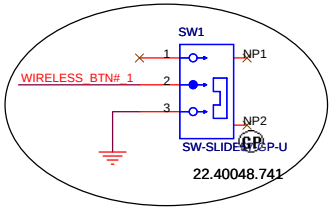
LA14_SA

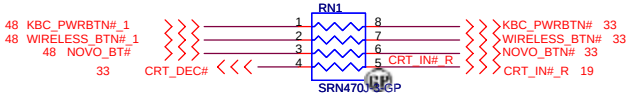
0205 ADD signal NOVO_BT#

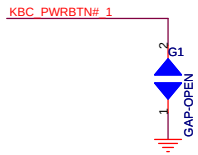
LA14_SA

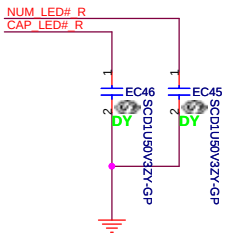
0205 modify POWERCN1 from 20.K0384.016 to 20.K0204.006

0223 modify POWERCN1 from 20.K0204.006 to 20.K0382.006









LA14_SA

0205 remove EC49

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Power Board**	
Size	Document Number **LA14**	Rev SB
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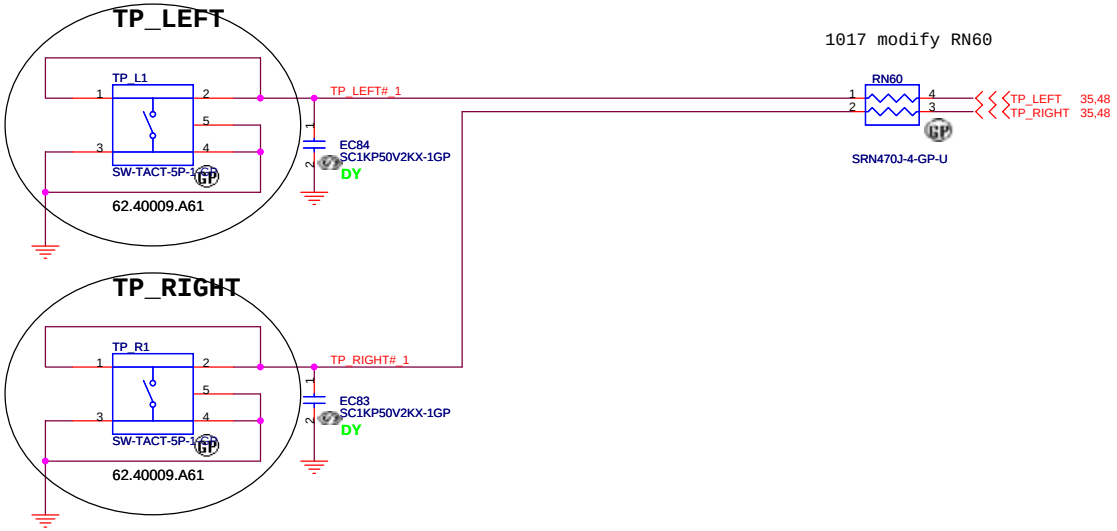
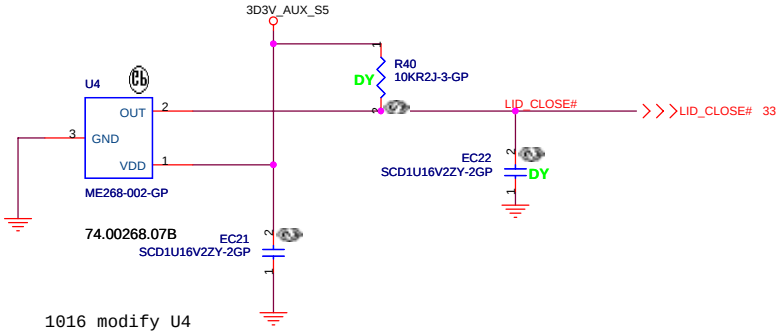


1017 modify RN60

1

1226 modify TP_L1 and TP_R1

Cover Up Switch



1016 modify U4

1017 modify U4

1017 add U61,R52,EC24 and EC23

1020 delete U61,R52,EC24 and EC23

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**SWITCHS**	
Size	Document Number **LA14**	Rev SB
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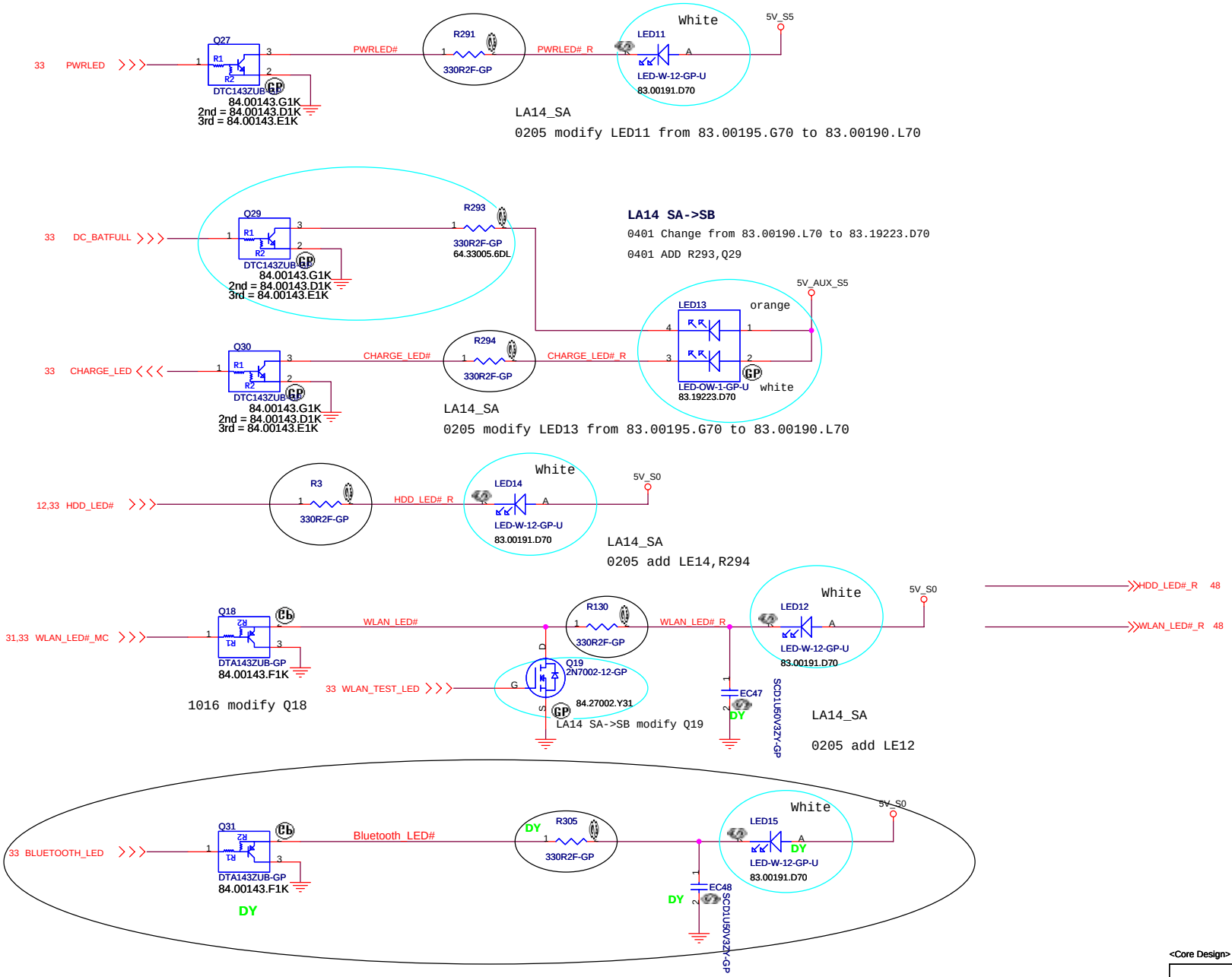

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

Size | Document Number: LA14 | Rev: SB

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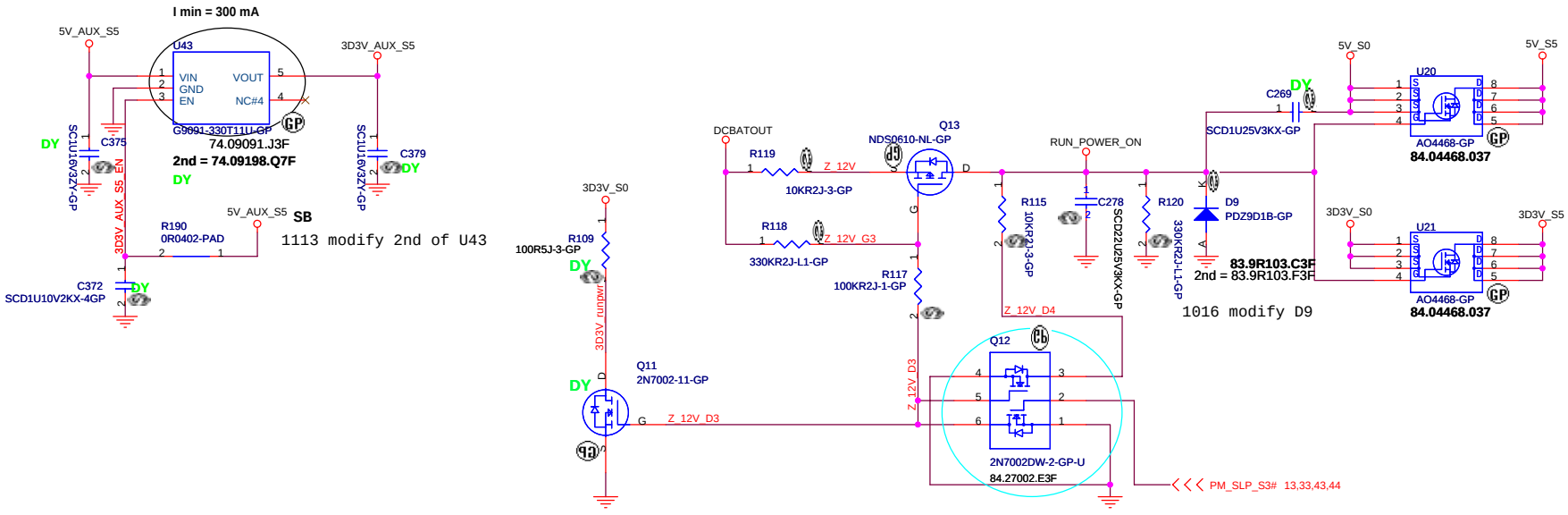
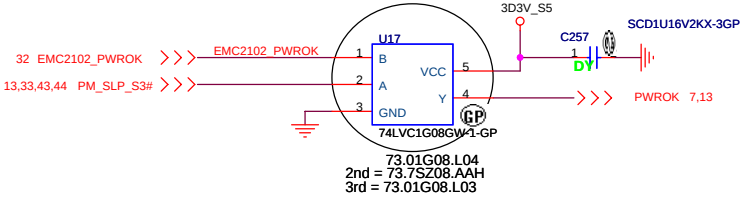
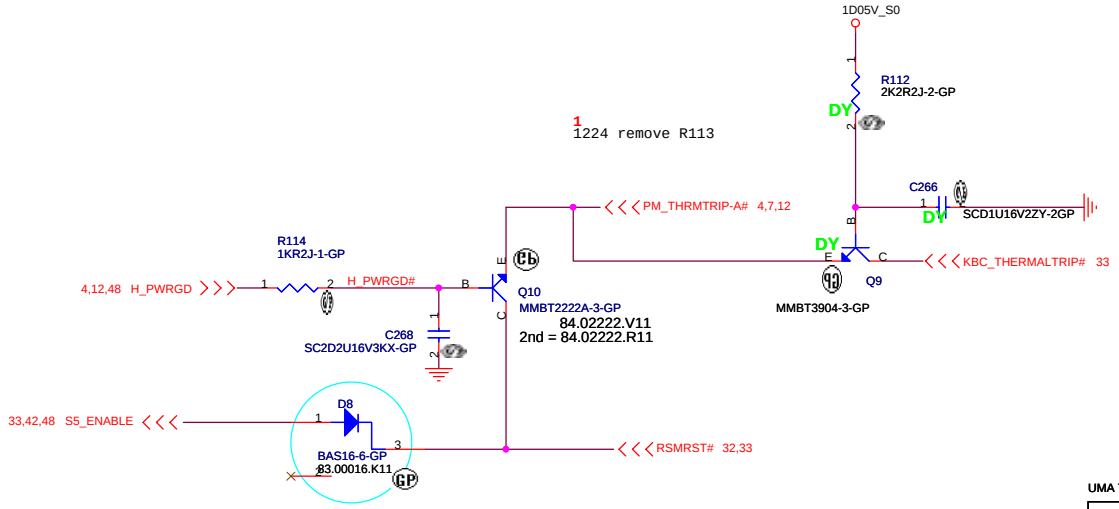
Aux Power 3D3V_AUX_S5

Run Power



LA14 SA->SB
0403 Change Q12 from 84.27002.D3F to 84.27002.E3F





LA14 SA->SB
0403 Change D8 from 83.00016.B11 to 83.00016.K11

UMA Two Phase

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
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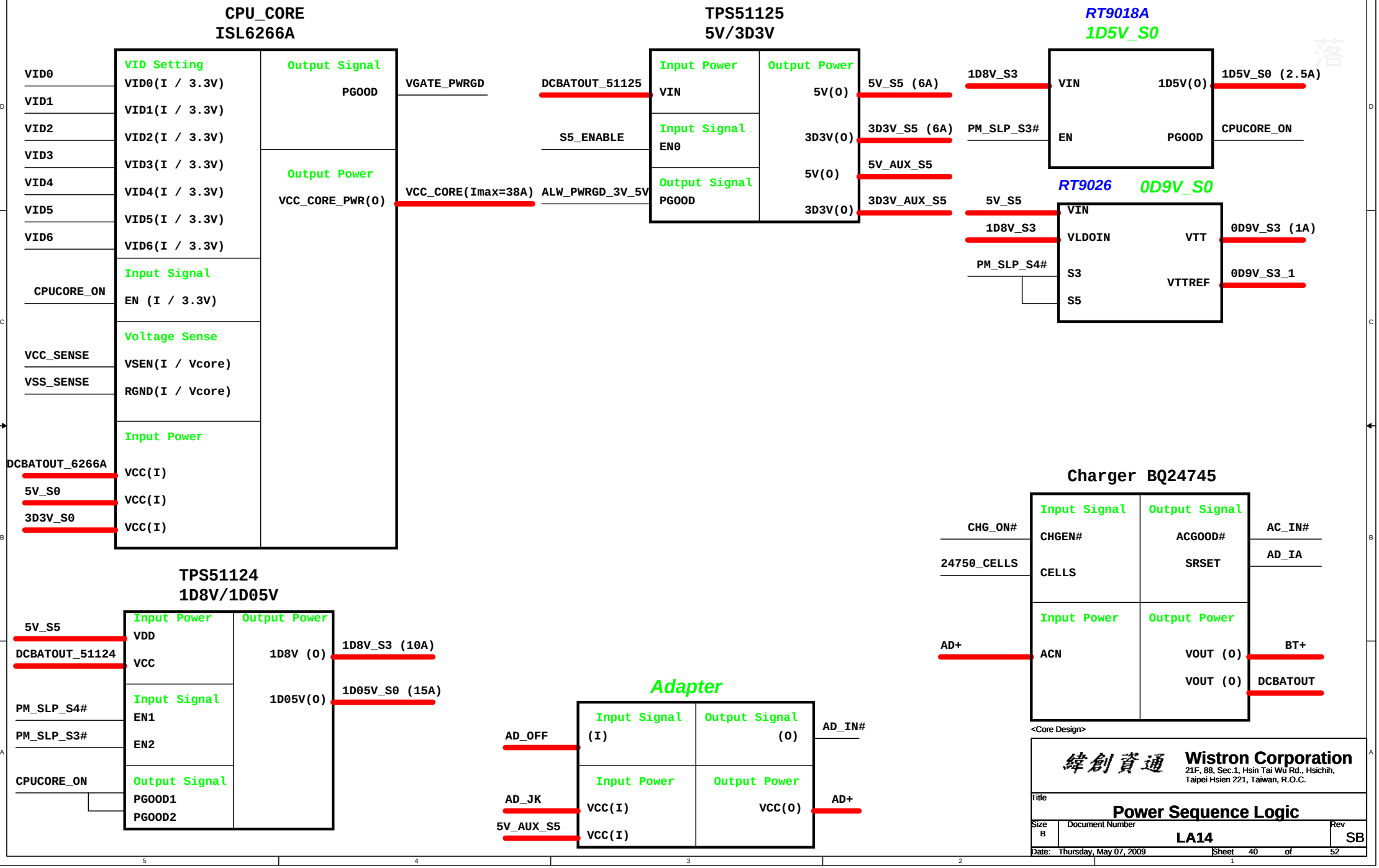
CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
TPS51125
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D5V_S0
VIN
EN
1D5V(O)
PGOOD
1D8V_S3
PM_SLP_S3#
1D5V_S0 (2.5A)
CPUCORE_ON
RT9026
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S4#
0D9V_S3 (1A)
0D9V_S3_1
Charger BQ24745
Input Signal
CHGEN#
CELLS
Input Power
ACN
Output Signal
ACGOOD#
SRSET
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
24750_CELLS
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D8V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D8V_S3 (10A)
1D05V_S0 (15A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
LA14
Rev
SB
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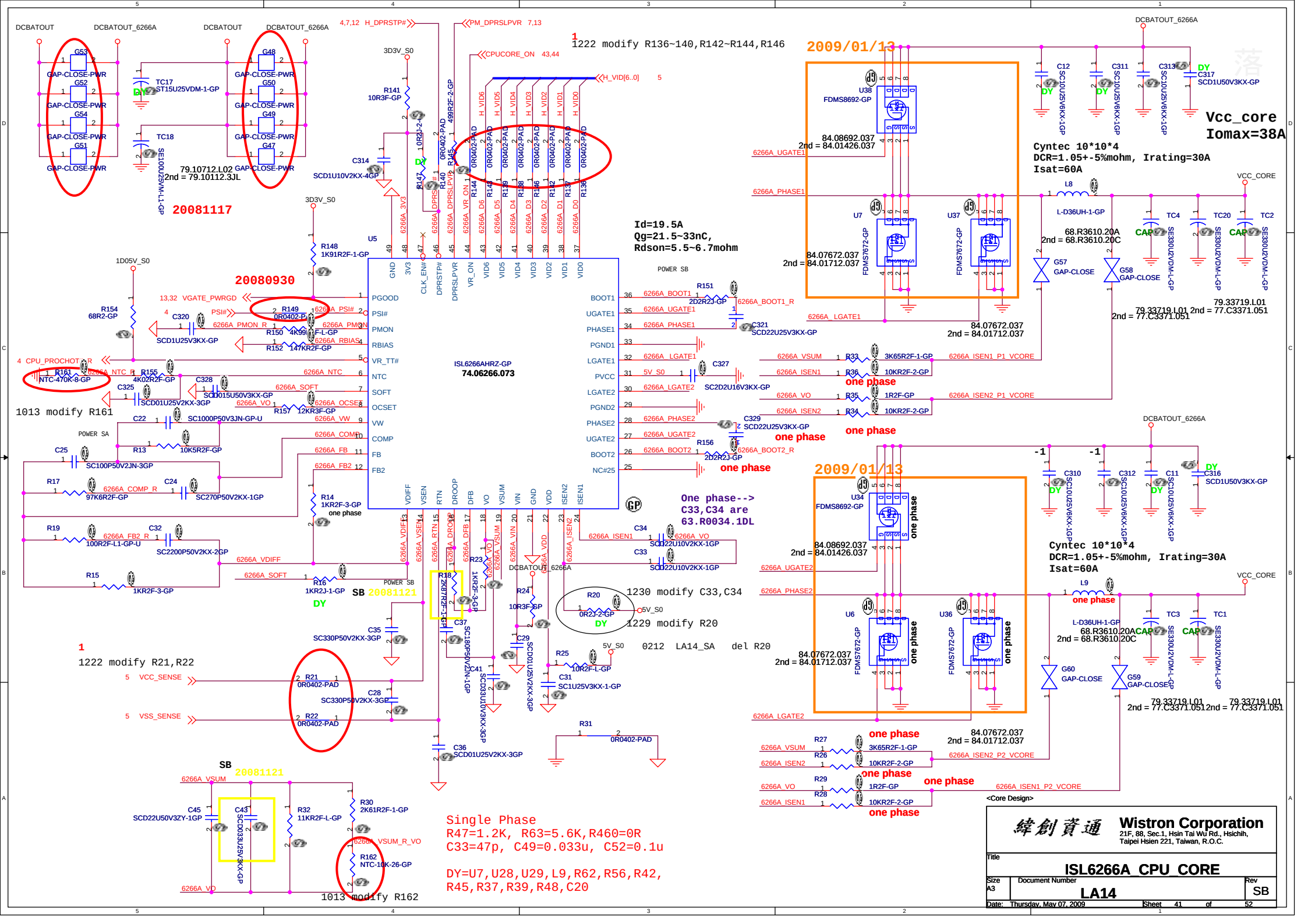
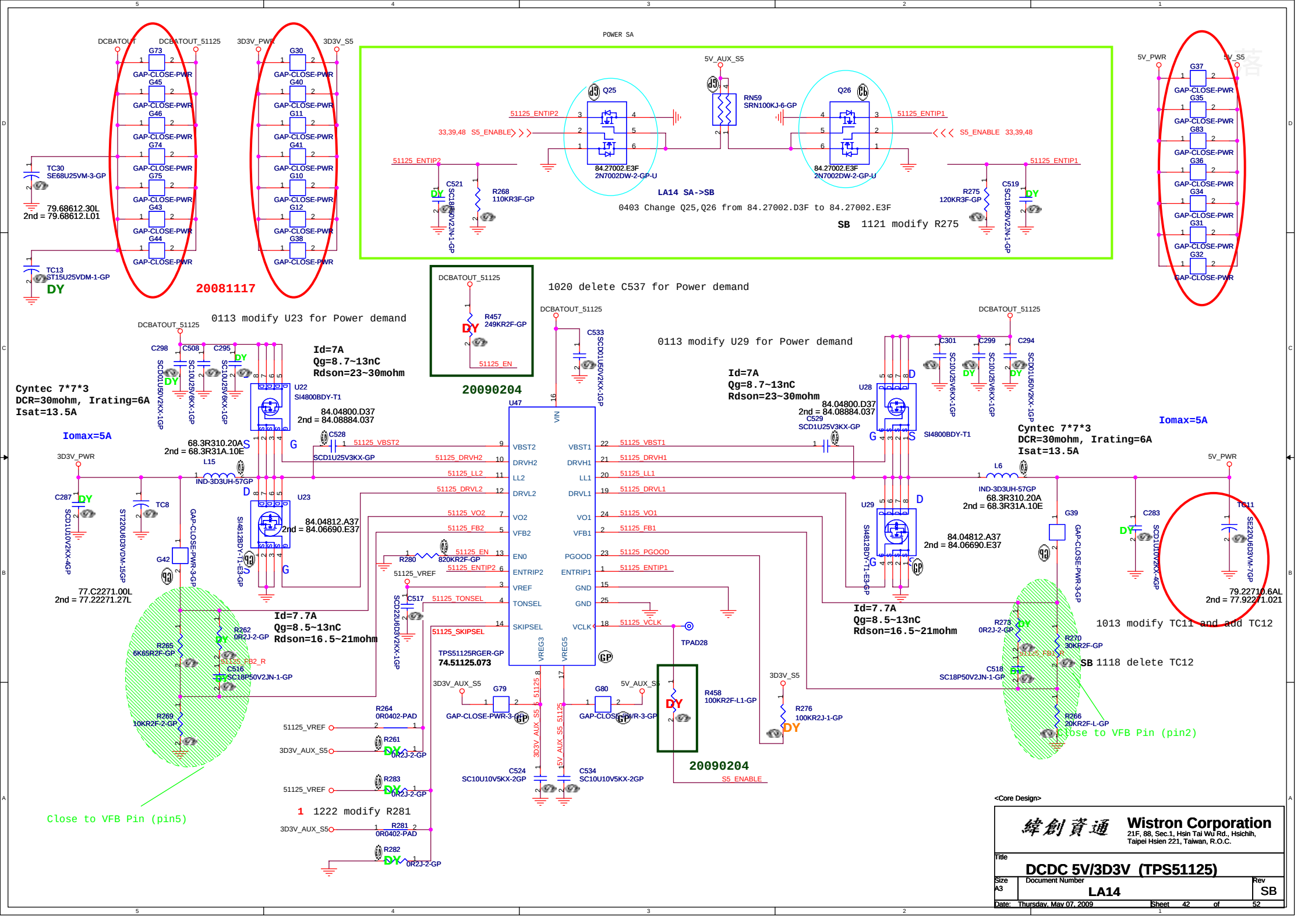

1222 modify R136~140,R142~R144,R146
2009/01/13
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
20081117
20080930
ISL6266AHRZ-GP
74.06266.073
1013 modify R161
one phase
One phase-->
C33,C34 are
63.R0034.1DL
1230 modify C33,C34
1229 modify R20
0212 LA14_SA del R20
SB 20081121
1222 modify R21,R22
1013 modify R162
Single Phase
R47=1.2K, R63=5.6K,R460=0R
C33=47p, C49=0.033u, C52=0.1u
DY=U7,U28,U29,L9,R62,R56,R42,
R45,R37,R39,R48,C20
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number
LA14
Rev SB
Date: Thursday, May 07, 2009
Sheet 41 of 52



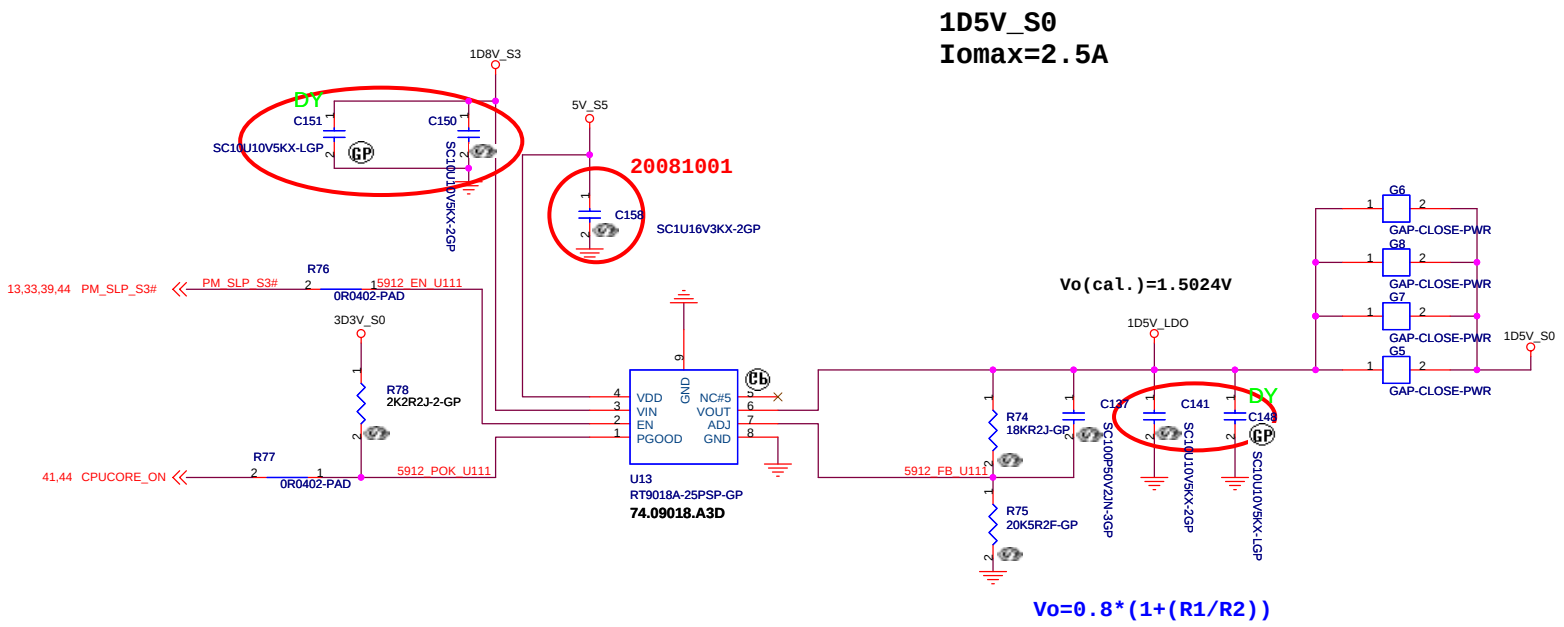
<Core Design>

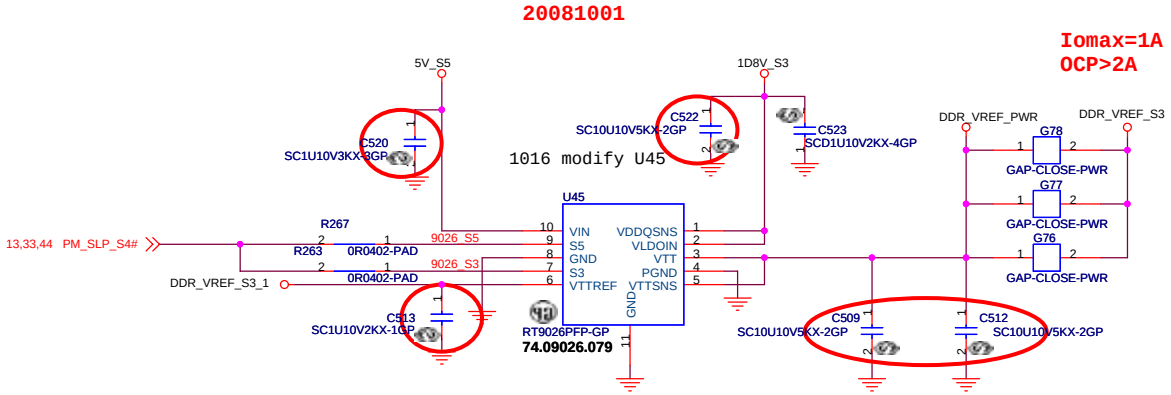
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)

Size: A3 | Document Number: LA14 | Rev: SB

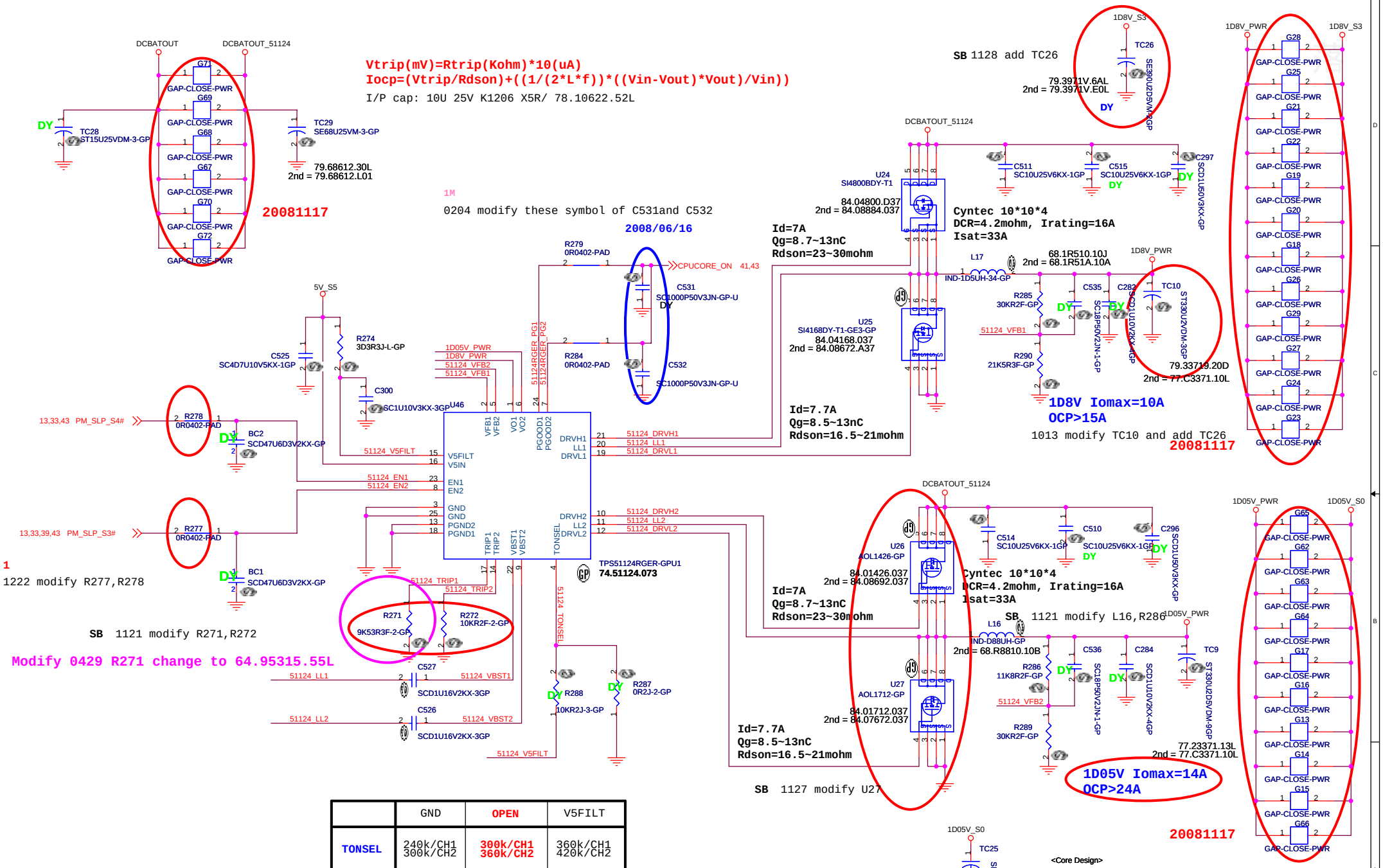
Date: Thursday, May 07, 2009 | Sheet 42 of 52





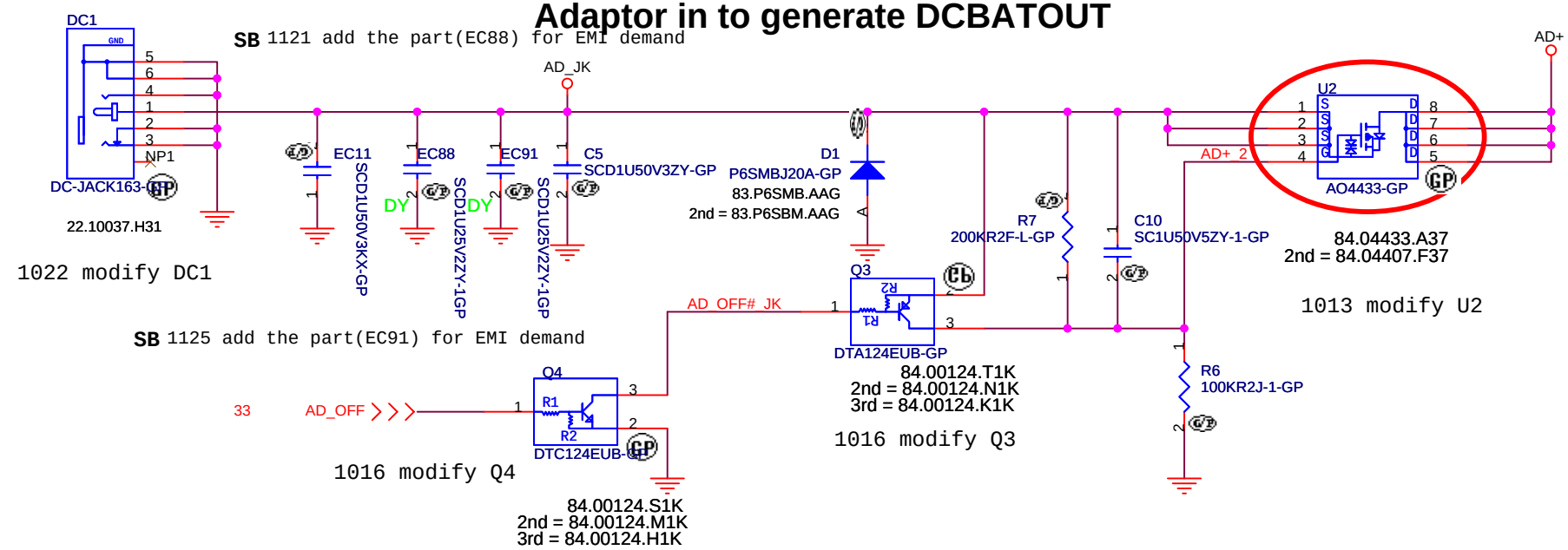
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**1D5V & 0D9V**
Size A3 / Document Number	**LA14**
Rev	SB
Date: Thursday, May 07, 2009	Sheet 43 of 52



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

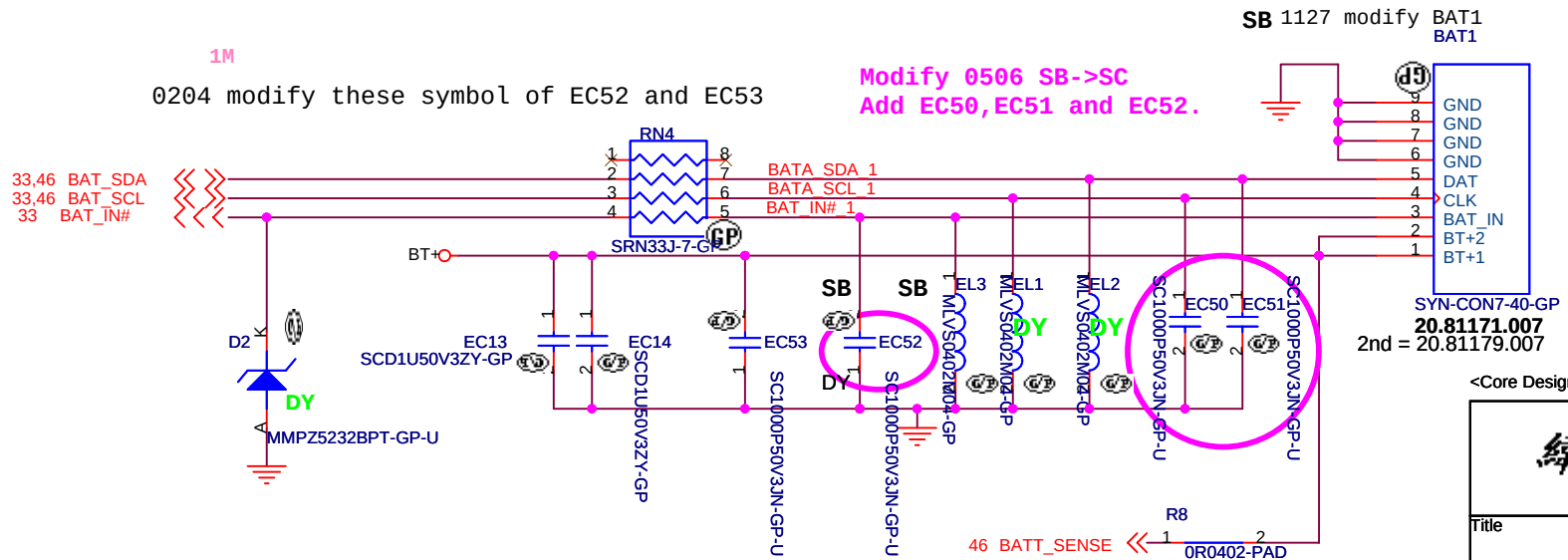
Adaptor in to generate DCBATOUT



LA_SA 0216 Change DC1 from 22.10037.F11 to 22.10037.H31

BATA_SDA_1 48
BATA_SCL_1 48
BAT_IN#_1 48

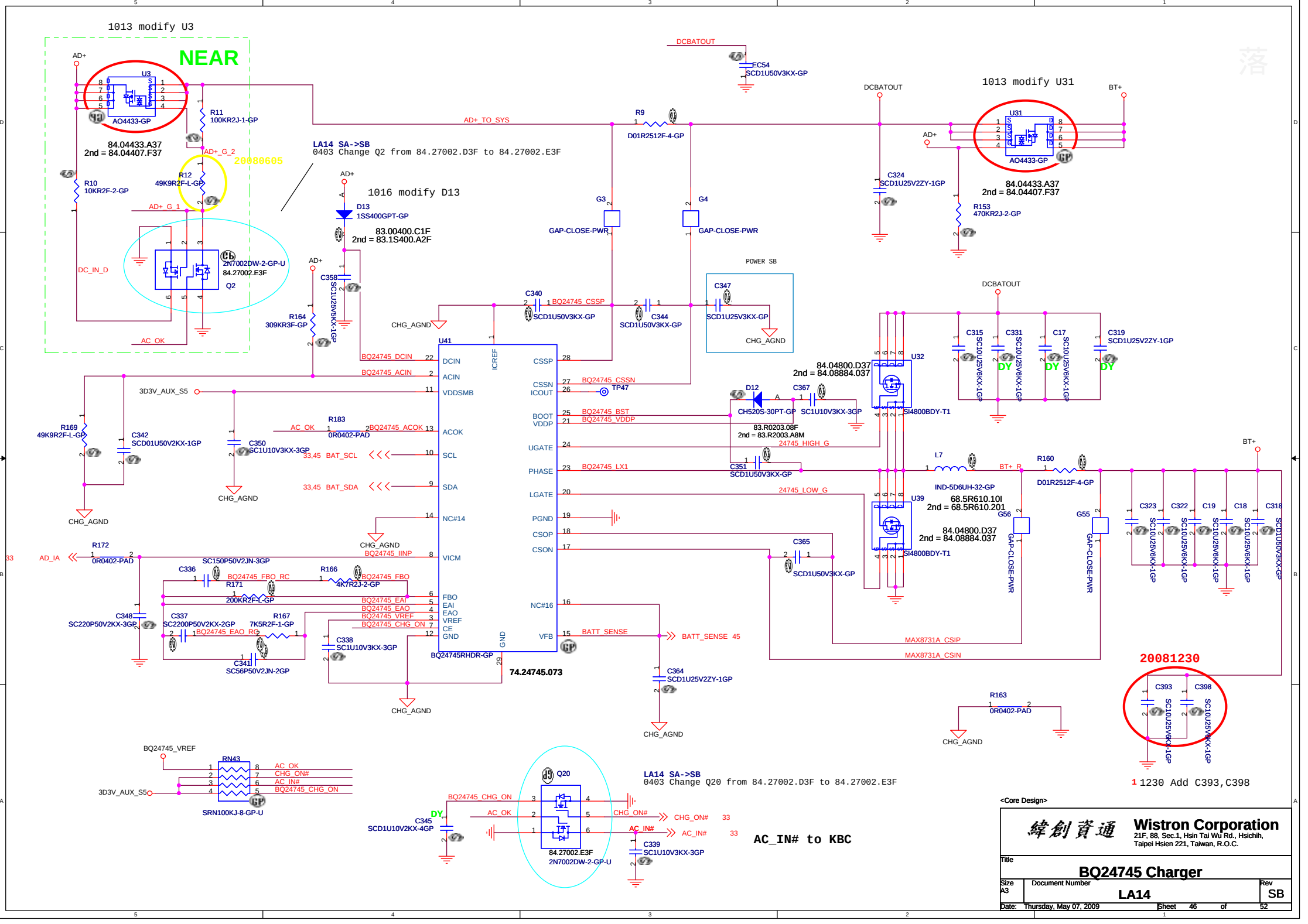
BATTERY CONNECTOR



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
Size	Document Number	Rev
	LA14	SB
Date: Thursday, May 07, 2009	Sheet 45 of 52	


1013 modify U3
NEAR
AD+
U3
AO4433-GP
84.04433.A37
2nd = 84.04407.F37
R11
100KR2J-1-GP
AD+_G_2
20080605
R12
49K9R2F-L-GP
R10
10KR2F-2-GP
AD+_G_1
DC_IN_D
2N7002DW-2-GP-U
84.27002.E3F
Q2
AC_OK
AD+_TO_SYS
R9
D01R2512F-4-GP
DCBATOUT
EC54
SCD1U50V3KX-GP
LA14 SA->SB
0403 Change Q2 from 84.27002.D3F to 84.27002.E3F
1016 modify D13
D13
1SS400GPT-GP
83.00400.C1F
2nd = 83.1S400.A2F
C358
SC1U25V5KX-1GP
R164
309KR3F-GP
G3
G4
GAP-CLOSE-PWR
POWER SB
C347
SCD1U25V3KX-GP
CHG_AGND
C340
SCD1U50V3KX-GP
BQ24745_CSSP
C344
SCD1U50V3KX-GP
U41
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
DCIN
ACIN
VDDSMB
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
BQ24745RHDR-GP
74.24745.073
BQ24745_CSSN
TP47
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BATT_SENSE
BATT_SENSE 45
R169
49K9R2F-L-GP
C342
SCD01U50V2KX-1GP
C350
SC1U10V3KX-3GP
R183
0R0402-PAD
AC_OK
BQ24745_ACOK
33,45 BAT_SCL
33,45 BAT_SDA
R172
0R0402-PAD
AD_IA
SC150P50V2JN-3GP
C336
BQ24745_FBO_RC
R166
4K7R2J-2-GP
BQ24745_FBO
R171
200KR2F-1-GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C348
SC220P50V2KX-3GP
C337
SC2200P50V2KX-2GP
BQ24745_EAO_RC
R167
7K5R2F-1-GP
C338
SC1U10V3KX-3GP
C341
SC56P50V2JN-2GP
BQ24745_IINP
C364
SCD1U25V2ZY-1GP
C365
SCD1U50V3KX-GP
D12
CH520S-30PT-GP
C367
SC1U10V3KX-3GP
83.R0203.08F
2nd = 83.R2003.A8M
C351
SCD1U50V3KX-GP
U32
84.04800.D37
2nd = 84.08884.037
SI4800BDY-T1
U39
68.5R610.10I
2nd = 68.5R610.201
84.04800.D37
2nd = 84.08884.037
SI4800BDY-T1
L7
IND-5D6UH-32-GP
BT+_R
R160
D01R2512F-4-GP
G56
G55
GAP-CLOSE-PWR
MAX8731A_CSIP
MAX8731A_CSIN
1013 modify U31
U31
AO4433-GP
84.04433.A37
2nd = 84.04407.F37
C324
SCD1U25V2ZY-1GP
R153
470KR2J-2-GP
BT+
C315
SC10U25V6KX-1GP
C331
SC10U25V6KX-1GP
C17
SC10U25V6KX-1GP
C319
SCD1U25V2ZY-1GP
DY
C323
SC10U25V6KX-1GP
C322
SC10U25V6KX-1GP
C19
SC10U25V6KX-1GP
C18
SC10U25V6KX-1GP
C318
SCD1U50V2KX-GP
20081230
C393
SC10U25V6KX-1GP
C398
SC10U25V6KX-1GP
1 1230 Add C393,C398
R163
0R0402-PAD
BQ24745_VREF
RN43
SRN100KJ-8-GP-U
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
LA14 SA->SB
0403 Change Q20 from 84.27002.D3F to 84.27002.E3F
Q20
84.27002.E3F
2N7002DW-2-GP-U
C345
SCD1U10V2KX-4GP
CHG_ON#
AC_IN#
C339
SC1U10V3KX-3GP
AC_IN# to KBC
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number
LA14
Rev SB
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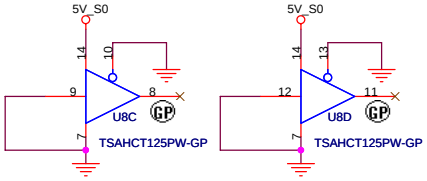
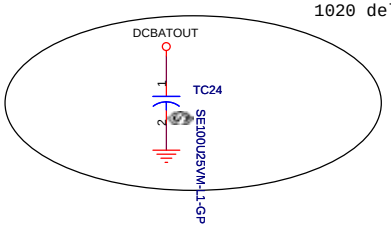
Sheet 46 of 52



73.74125.L13
2nd = 73.74125.L12

73.74125.L13
2nd = 73.74125.L12

1020 delete TC14,TC15

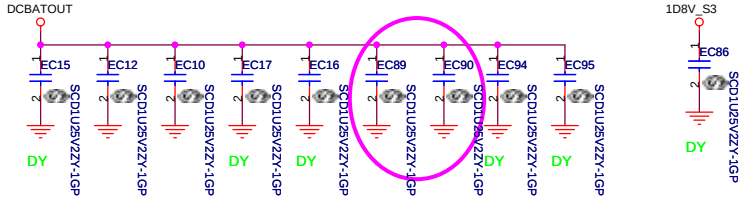


SB
1117 delete TC19

79.10712.L02
2nd = 79.10112.3JL

1016 modify U32

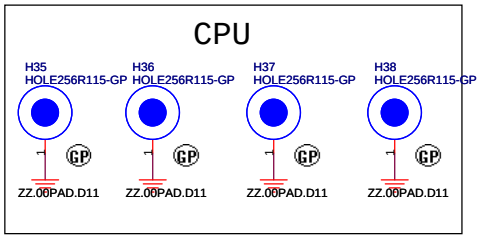
1017 add these parts(EC10,EC12,EC15~EC17,EC86) for EMI demand
1020 add the part(EC86) for EMI demand 1125 add the part(EC90) for EMI demand
SB 1121 add the part(EC89) for EMI demand 1128 add EC94,EC95 for EMI demand



Modify 0506 SB->SC
Add EC89 and EC90 for EMI demand

1016 add GND1 and GND2 for EMI demand
1017 add GND3 and modify GND2 for EMI demand

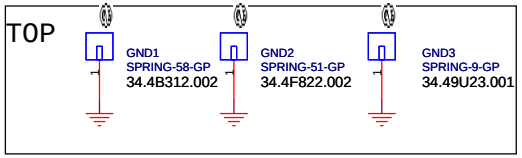
LA14 SA->SB
0401 DY GND9
0402 Del GND4,GND7,GND8,GND9



1016 modify H35~H38
1016 delete H9~H12

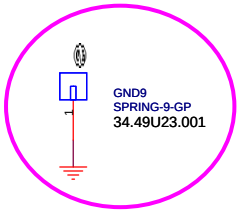
LA14 SB 0402 modify H35~H36

1016 modify H31 and H32
SB 1120 remove H31and H32



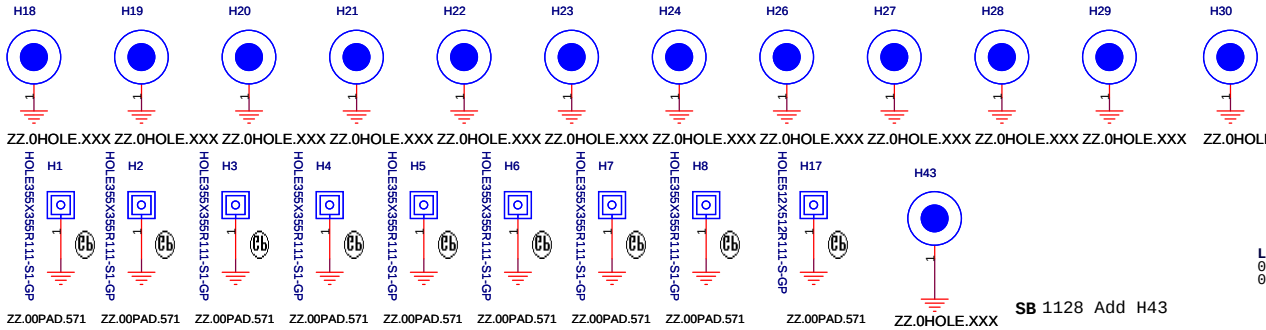
SB 1128 Add GND4,GND7,GND8

1 1230 Add GND9



Modify 0506 SB->SC
Add GND9 for EMI demand

LA_SA 0218 Change H35~H38 from ZZ.00PAD.571 to ZZ.00PAD.801

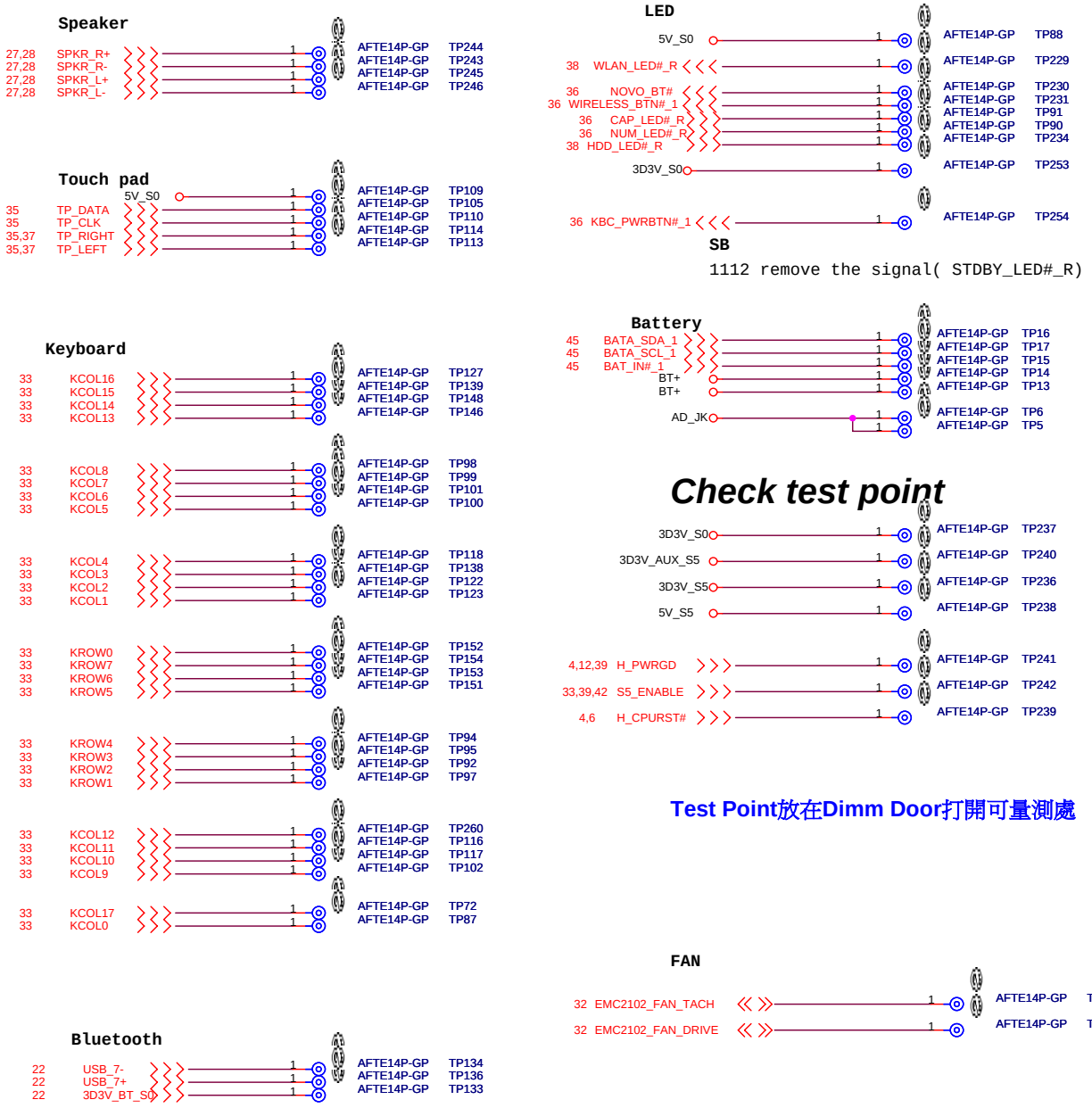


LA14 SA->SB
0401 DY H8
0402 Del H8

SB 1128 Add H43

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**EMI/Spring/Boss**	
Size	Document Number **LA14**	Rev SB
Date: Thursday, May 07, 2009	Sheet 47 of 52	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**AFTE test point**	
Size	Document Number **LA14**	Rev SB
Date: Thursday, May 07, 2009	Sheet 48 of 52	

0910 delete F4(Page 18)
0910 update footprint of U15(Page 30)
0910 delete RIGHT1 and LEFT1(Page 33)
0910 modify net names of TP_LEFT and TP_RIGHT(Page 36)
0910 modify test points of AFTE and TPAD
0911 modify net name from LPC_RST to PLT_RST1#(Page 24)
0911 add net name(RBIAS,LED_DUPLEX#,SMDATA,SMCLK)(Page 24)
0911 add net name(DVDD_1_8,ACZ_SDATAIN0_R,FLY_P,FLY_N,VREF_LO,VREF_HI)(Page 26)
0911 add net name(EAPD#_R)(Page 27)
0912 modify the schematic of Page 33
0912 delete GMCH_TXB*(Page 7& 18)
0912 add these parts for EMI demand(page 7,18,20,21,23,26,28,29,30,32,33,34,35)
0915 modify net name from 10M/100M/1G_LED# to 10M/100M_LED#(page24,25)
0915 delete these parts for EMI demand(page 30)
0915 add EC34 for EMI demand(page3)
0915 add EC73 for EMI demand(page 12)
0915 modify LEDs port
0916 move net(SPI_WP#) from U9 pin120 to pin25(page33)
0930 modify BLUE1(page22)
0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)
0930 modify FAN1(page32)
0930 modify TPAD1(page35)
0930 modify KB1(page33)
0930 modify net name for BIOS demand(page33)
1001 delete these parts for EMI demand(ED1~8)
1009 modify net name for GND to AGND(page27)
1009 add R4,R5 for AC decopling(page27)
1009 add R96(page30)
1013 modify TPAD1(page35)
1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)
1013 modify TC11 and add TC12(page42)
1013 modify TC10 and add TC26(page44)
1013 modify U2(page45)
1013 modify U3 and U31(page 46)
1013 modify R161 and R162(page41)
1013 modify card1(page 30)
1014 modify these LEDs(LED11,LED12)(page38)
1014 modify these nets(page 26)
1014 modify R258 from 10k to 20k ohm(page26)
1014 add ER5 for EMI deamnd(page3)
1015 modify LCD1 pin define(page 18)
1015 modify the power from 3D3V_S5 to 5V_S5(page38)
1015 modify TPAD1(page35)
1015 modify RN57(page28)
1015 modify F1(page18)

1016 modify L1,L2 and L3(page 19)
1016 modify XF1(page 25)
1016 modify RN53 and U10(page 24)
1016 modify U8(page19,47)
1016 modify U4(page 37)
1016 modify U23(page 43)
1016 modify X2(page12)
1016 modify X1(page 33)
1016 modify X3(page 3)
1016 modify D13(page 46)
1016 modify D23(page 20)
1016 modify D9(page 39)
1016 modify D4(page 19)
1016 modify Q3 and Q4(page45)
1016 modify Q18(page 36)
1016 modify Q15~Q17(page 36)
1016 modify Q27~Q30(page38)
1016 modify Q6 and Q14(page 32)
1016 modify Q8(PAGE 24)
1016 add GND1 nad GND2 for EMI demand(page 47)
1016 modify LCD1 pin define(page 18)
1016 delete H9~H12 and modify H35~H38,H31,H32(page 47)
1017 add these parts for EMI demand(page 47)
1017 delete these parts(EC208~EC210)(page 7)
1017 modify BLUE1(page 22)
1017 modify FAN1(page 32)
1017 modify R291 and R293(page 38)
1017 add U61,R52,EC23 and EC24(page 37)
1017 modify RN60(page37)
1017 add TC25(page 44)
1017 add GND3 and modify GND2 for EMI demand(page 47)
1017 modify USB signal connection(page13,18,22,23,30,31,48)
1020 delete C537 for Power demand(page42)
1020 add the part(EC86) for EMI demand(page 47)
1020 delete U61,R52,EC24 and EC23(page 37)
1020 delete TC14,TC15(page 47)
1021 modify TC16(page 31)
1021 delete TC23(page 23)
1021 modify TC5(page 20)
1021 modify and swap these parts(USB1 and USB2)(page 23)
1021 modify SATA1(page 20)
1022 modify DC1(page 45)

SA to SB

1106 modify net connection of RN46 and RN44(page33) for layout demand
1106 modify LED11 and LED12(page38) for fixing issue
1106 modify LED power from 5V_S5 to 5V_AUX_S5(page38) for customer demand
1112 remove the signal(STDBY_LED#_FR)page38 for customer demand
1112 remove these signals(STDBY_LED#_FR and STDBY_LED#_R) and R131(page36) for customer demand
1112 remove the signal(STDBY_LED#_R)page36 for customer demand
1112 remove the signal(STDBY_LED#_R)and TP253(page48) for customer demand
1113 modify C103 and C106(page24) for crystal issue
1113 modify 2nd of U19(page26)
1113 modify 2nd of U43(page39)
1113 modify 2nd of U44(page10)
1113 modify U48(page22)
1117 delete MDC function(R231,R237,R232,R234)(page12)
1117 delete TC19(page 47) for ME deamnd
1118 modify PCB Ver. from SA to SB(page33)
1118 delete TC12(page42) for layout demand
1118 delete TC27(page9) for layout demand
1118 delete R107 and add L18 for cost down
1119 modify R130 and R133(page 36) for LED brightness
1119 modify EC52 and EL3(page45) for EMI demand
1119 modify SPK1(page 28) for ME deamnd
1119 add G84 for RTC reset demand
1120 modify EC78for EMI demand((page10)
1120 modify PowerCN1 pin3 and remove EC44(page36) fro LED function
1120 remove H31 and H32(page47)for ME demand
1120 add RN61 and RN62(page3) for layout demand
1120 swap these nets(CLK_MCH_3GPLL,CLK_MCH_3GPLL#, CLK_PCIE_MINI1,CLK_PCIE_MINI1#)(page3)for CLK REQ demand
1120 add the net(SATACLKREQ#)(page3,13)for CLK REQ demand
1120 move these nets (CLK_PCIE_MINI1,CLK_PCIE_MINI1#)(page3)for CLK REQ demand
1120 modify RN61 and RN62(page3)for CLK REQ demand
1121 add EC87 for EMI demand(page18)
1121 add the part(EC89) for EMI demand(page47)
1121 add the part(EC88) for EMI demand(page45)
1121 modify R18,C43(page41) for Power demand
1121 modify R275(page42)for Power demand
1121 modify R271,R272,R286 and L16(page44) for Power demand
1124 modify U42 and delete R182,R185 (page32) for thermal function
1124 modify these names of these nets(G7922_SGND2,G7922_SGND3...) (page32) for thermal function
1124 add R302(page3) for clock gen function
1125 add the part(EC90) for EMI demand(page47)
1125 add the part(EC91) for EMI demand(page45)
1125 modify R125,R126(page18) for LCD brightness control
1125 modify RN40 and delete RN42(page32) for layout demand
1125 add EC92 and EC93 for EMI demand(page 22)
1126 add these nets (PCIE_REQ_LAN#,PCIE_REQ_MINI#)(page3)for CLK REQ demand
1126 delete R230,R233,R235,R236 and RN63(page12) for removing MDC function
1126 add C541 and modify R101(page26) for codec function
1126 modify RN61 and RN62(page3) for layout demand
1126 modify EU1,EU2 and add EU3,EU4 for EMI demand(page28)
1127 modify CRT1(page19) for customer demand
1127 swap the nets of RN61 and RN62 for layout demand(page3)
1127 modify BAT1(page45) for ME demand
1127 modify U27(page44) for power demand
1127 modify C377(page32) for thermal function
1128 Add H43,GND4,GND7,GND8(page47) for EMI demand
1128 modify LCD1(page18) for cost down
1128 Add L19(page24) for vender demand
1128 add EC94,EC95 for EMI demand(page47)
1201 modify C3 (page18)
1201 modify EC6~9(page28)
1204 modify RN36
1204 modify second source of RJ1

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Change List**	
Size	Document Number **LA14**	Rev SB
Date: Thursday, May 07, 2009	Sheet 51 of 52	

SB to 1

1222 modify U42 for customer demand(page32)
1222 modify these names of nets (BMC2102_DN2,DP2,DN3,DP3,PWROK,FAN_TACH,FAN_DRIVE)(page32)
1222 modify RN58 from 68 to 56 ohm for customer demand(page28)
1222 modify PCB Ver. from SB to -1(page33)
1222 modify TC5 for HDD side(page20)
1222 modify card1 from 20.I0043.001 to 20.I0043.011for CE demand(PAGE30)
1223 modify the net(EMC2102_CLK_SEL) for reducing component (page32)
1223 modify the net(RSMRST#) for reducing component(page33)
1224 dummy C6(page27)
1224 add R306 for FSB Dynamic ODT(dummy)(page7)
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<Core Design>

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